Build–up/Bump–less Ultra–thin Wafer Stacking Technology without Carrier Wafer

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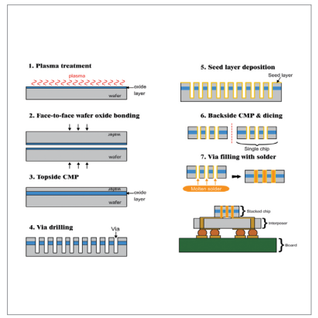


Improve 3D package yield by stacking ultra–thin wafers with the build–up method

Client / Market

- Semiconductor manufacturer (Foundry, Fabless, Assembly)

Necessity of this Technology

- When manufacturing stacking package, there are handling, yield, productivity issues in stacking ultra–thin wafers.
- Existing technology for fabricating an ultra–thin chip bonds the thin wafer temporarily to the carrier wafer to prevent damage and proceeds with follow–up process, and the process cost is high. Since bonding and stacking using a bump by chip unit, yield and productivity is low.
- Mobile AP and other semiconductor packages are becoming high performance, light weight, and thin and small.
- Currently used 2D interconnection package manufacturing method has reached technical limits regarding scaling down to meet the consumer demand and stacking package technology is becoming popular as alternative technology.

Technical Differentiation

- Since the thin wafer is not bonded temporarily to the carrier wafer, and the ultra–thin wafer stacking package is manufactured with the build–up method, handling ultra–thin wafer becomes easy and yield improves.
- Producing wafer level stacking packages with the build–up method leads to high yield and mass production, and it can achieve fine pitch as it simultaneously realizes TSV and vertical interconnection bumplessly.
- Wafer level stacking method can easily handle and stack ultra–thin wafer without using additional carrier wafer and boasts higher yield and mass production compared to chip level stacking technology.
- Vertical interconnection of bumpless TSV can achieve fine pitch and secure bonding reliability.

Excellence of Technology

- The technology uses the lowermost device wafer without temporary bonding to additional carrier wafer to easily handle ultra–thin wafer and stacking with the build–up method to form interconnection of TSV.

DESIRED PARTNERSHIP

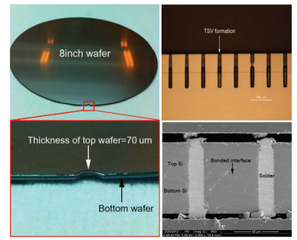
Technology Transfer | Licensing | Joint Research | Other

TECHNOLOGY READINESS LEVEL [TRL]

Research, basic explanation | Project concept or idea development | Technology idea verification | Prototype development | Trial product production/ evaluation in similar environment | Pilot field demonstration | Development and optimization of commercial model | Commercial product demonstration | Mass production and initial market launch

- The lowermost device wafer is used as the carrier, and bond and backgrind the wafer with the build–up method to thin the wafer from each layer.
- On multilayered wafers stacked with the method above, a through hole is created across the wafers, and using molten metal or plating method, form TSV interconnection on each layer without bumps.
- The head researcher has over 20 years of research experience.

Wafer Level Build–up Bumpless Stacking Technology



Current Intellectual Property Right Status

PATENT

- Semiconductor Chip Stacking Package and Manufacturing Method (KR1036441, PCT/KR2011/001166, SP201201174–8, US8722513)
- Semiconductor Chip Pickup Device (KR1186799)
- Semiconductor Chip Stacking Package and Manufacturing Method (KR1172533)
- Chip Stack and Interconnection Method using Electric Plating including the Chip, Stacking Chip and TSV for Chip Interconnection (KR1225253)
- Semiconductor Chip Stacking Package and Manufacturing Method (KR1036441)
- TSV for Semiconductor Device 3D Package and Manufacturing Method (KR1071993)
- TSV for Semiconductor 3D Package Using Electroplating and Manufacturing Method (KR1049380, US8513061)
- Chip Stacking Method Using Insulating Film, Chip Stacked with the Method, Insulating Film for the Method and Manufacturing Method (KR1242281)
- Manufacturing Method for TSV for Semiconductor Device 3D Package (KR1103275)

KNOW–HOW

- Void free wafer direct bonding technology
- Wafer surface pre–treatment technology
- Bumpless TSV (Through–Silicon Via) formation and ultra–thin wafer build–up stacking technology