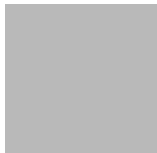




Helmut Schift :: Head Polymer Nanotechnology Group :: Paul Scherrer Institut

More (than Moore) applications based on nanoimprint lithography

IFAME 2016, Daejeon, Korea, August 18, 2016



20 Years of Nanoimprint lithography (NIL)

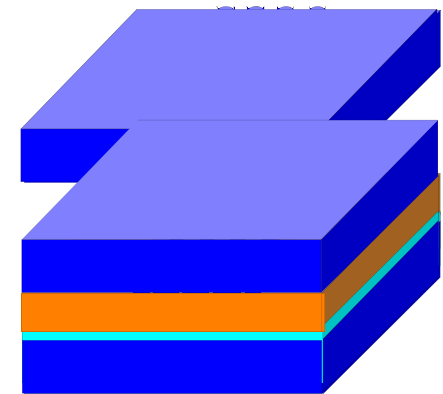
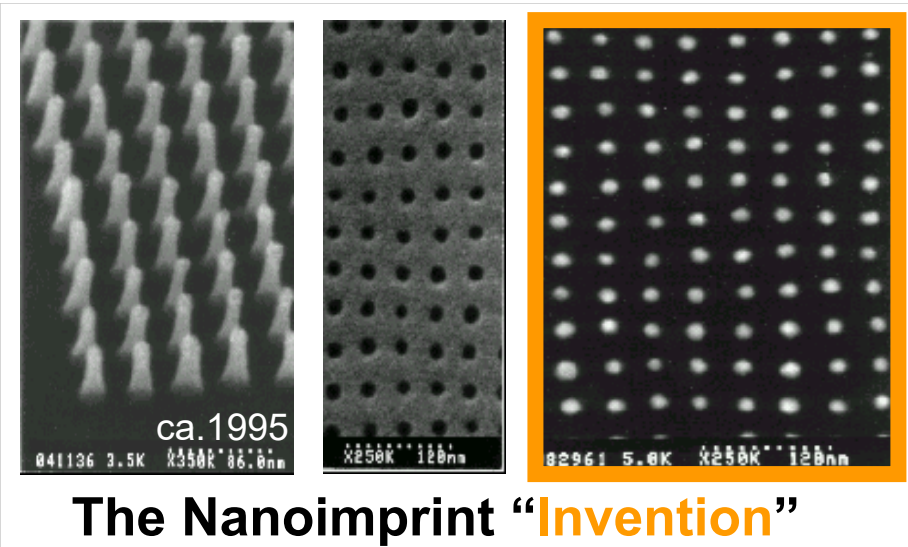


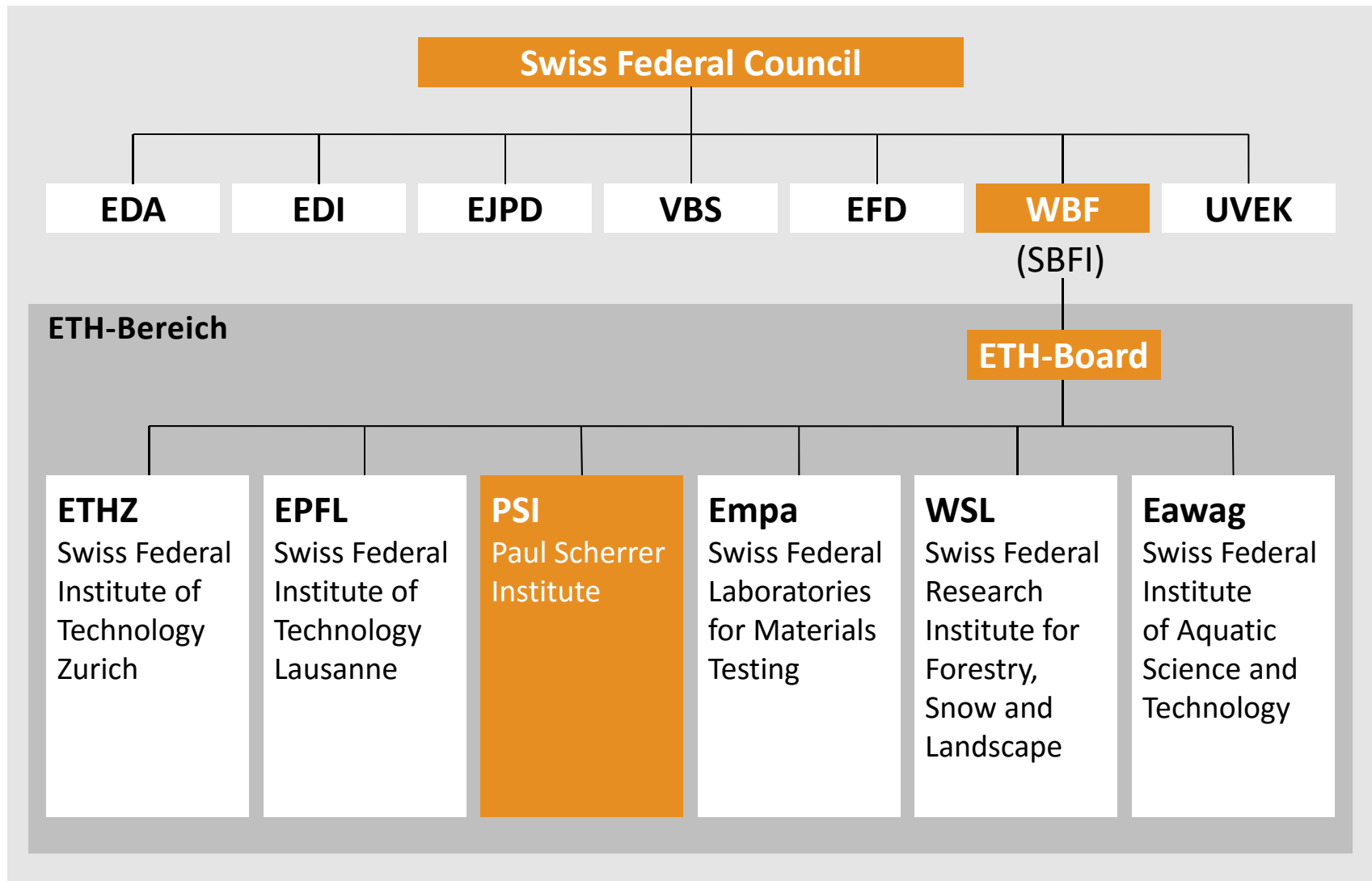
**PRINCETON
UNIVERSITY**
Applied Physics A
Materials Science & Processing

Stephen Y. Chou, Princeton

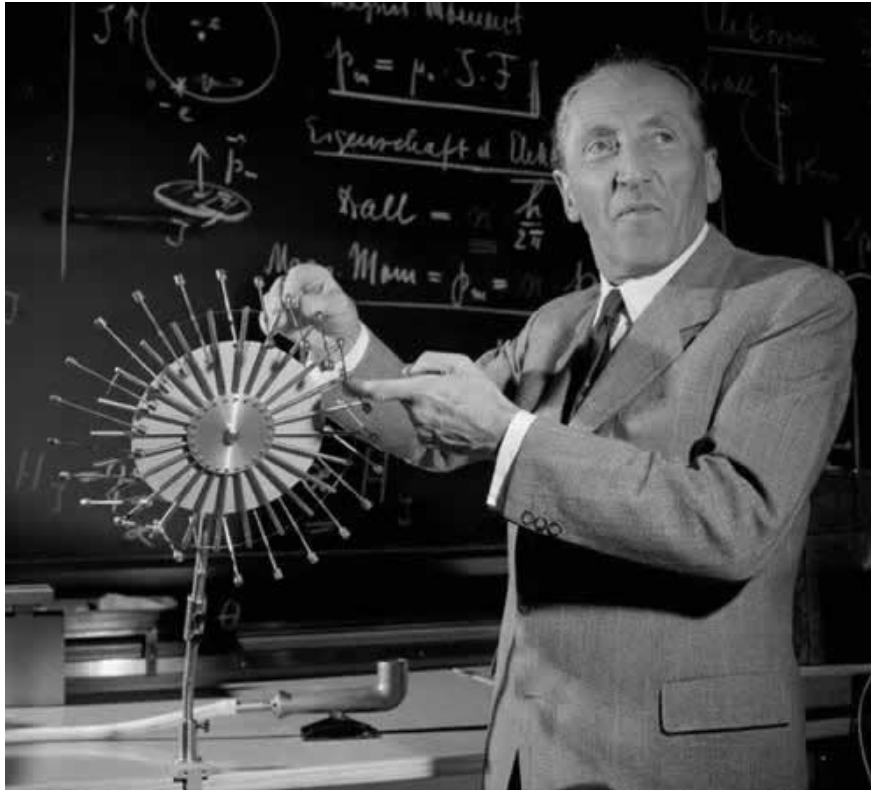
“Until 20 years ago, nanolithography by a mechanical method was unthinkable. Not only do mechanical methods use a completely different physical principle from the traditional lithography [wave/particle interactions (e.g., photons, electrons) with matter]; but also mechanical methods were perceived, at that time, to be applicable only for large scale structures, not for nanoscale.”

Appl. Phys. A (2015) 121:317–318





Paul Scherrer (1890–1969)



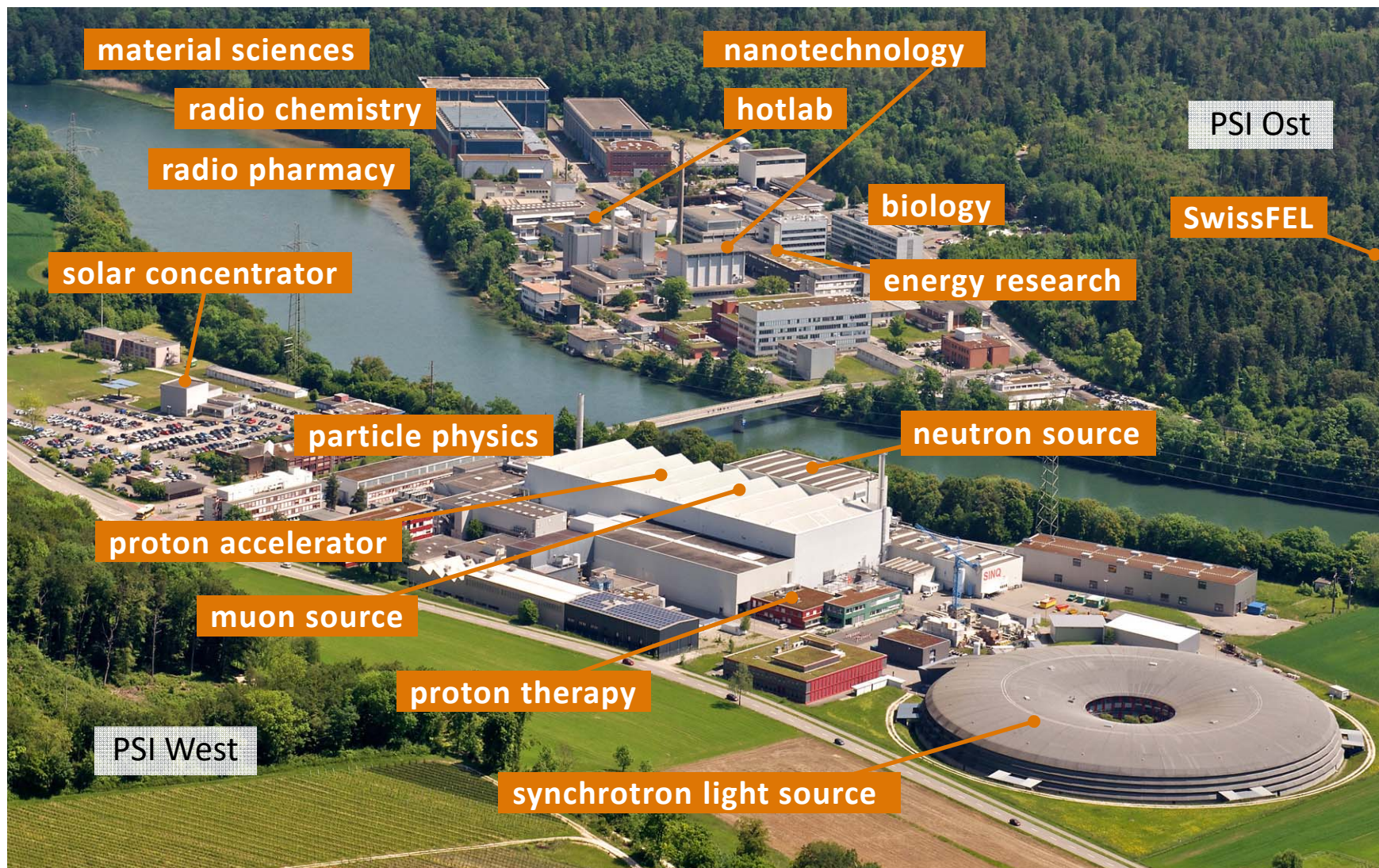
- Physics and mathematical studies at ETH Zürich, at Königsberg and Göttingen (Germany)
- 1920: professorship in experimental physics at ETH Zürich, from 1927 director of Physikalisches Institut. Known for his excellent lectures
- Research into X-ray scattering on crystals, liquids and gases. Later research focus: nuclear physics
- 1946: president of the Schweizerische Studienkommission für Atomenergie
- involved in the foundation of CERN

← Basel

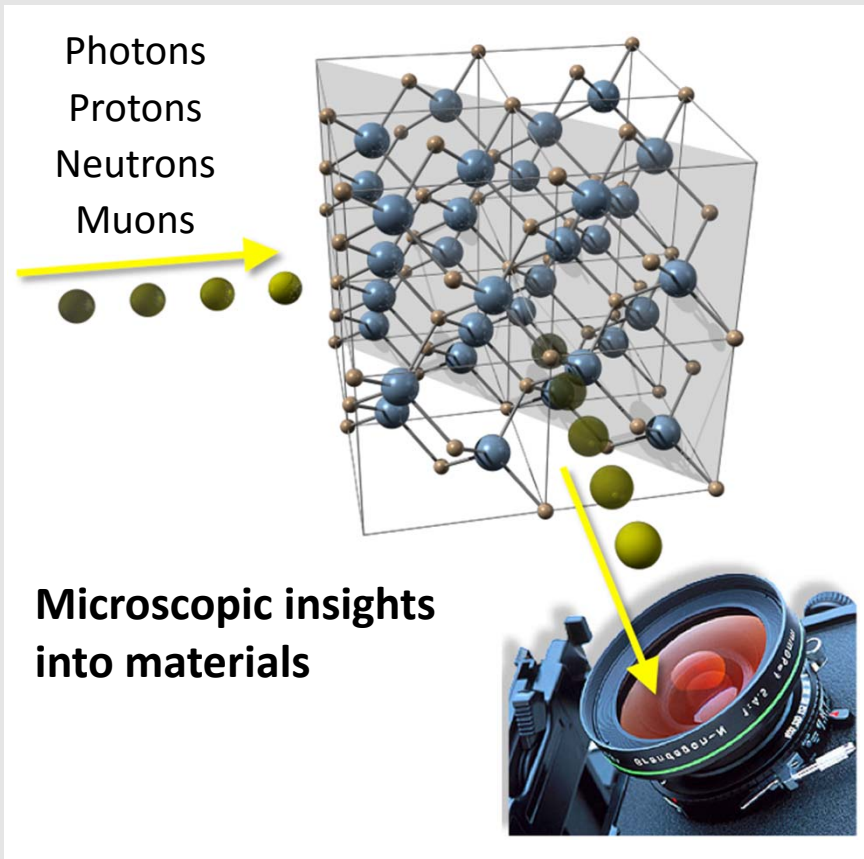
Germany ↑

Aarau/Bern ↓

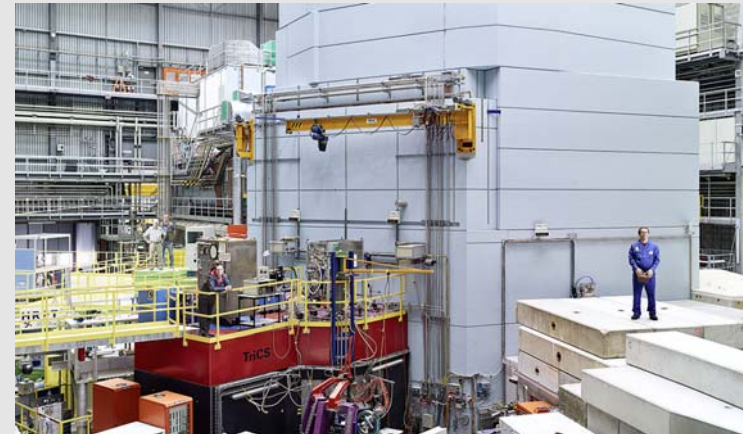
Zürich →



Research at large facilities



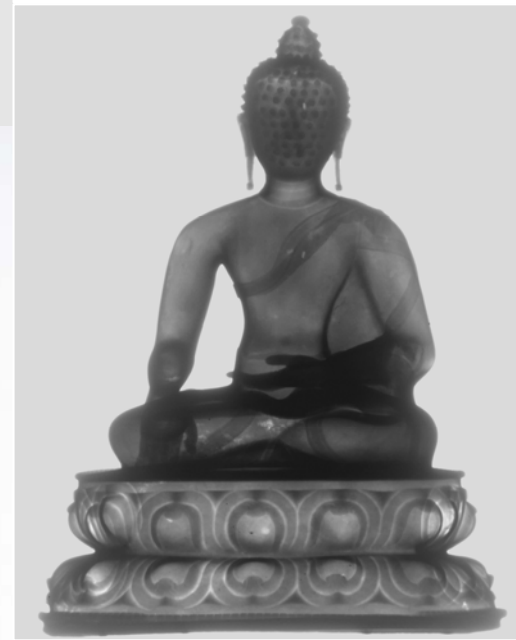
Synchrotron lightsource SLS
Neutron source SINQ
Muon source SpS



Neutron Radiography



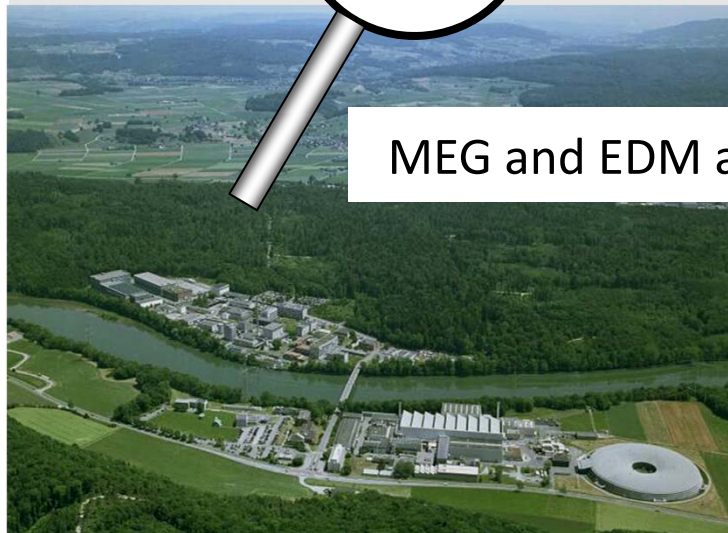
X-rays



Are there any physics beyond our standard models?

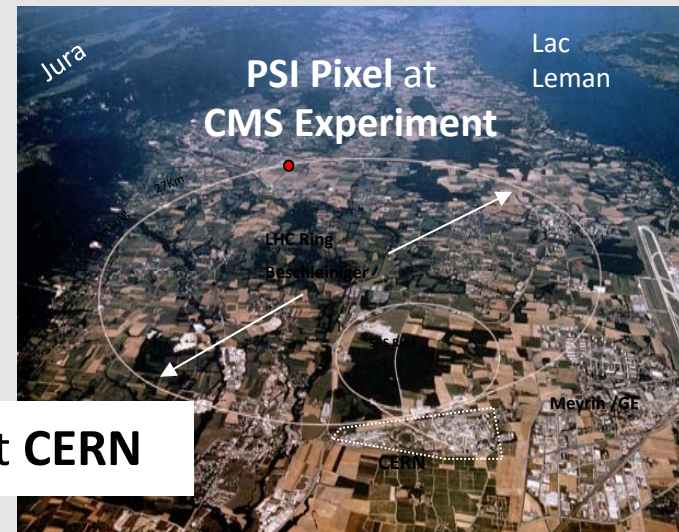
New particles? New forces?

extreme **prec**ision



MEG and EDM at **PSI**

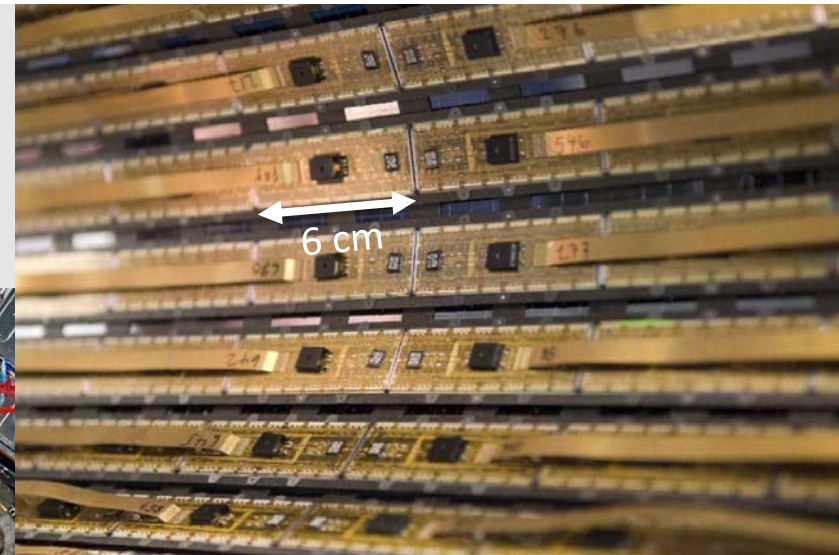
extreme energies



LHC at **CERN**

LHC: CMS Detector co-developed at PSI

The pixel detector played a mayor role in the discovery of the Higgs particles.

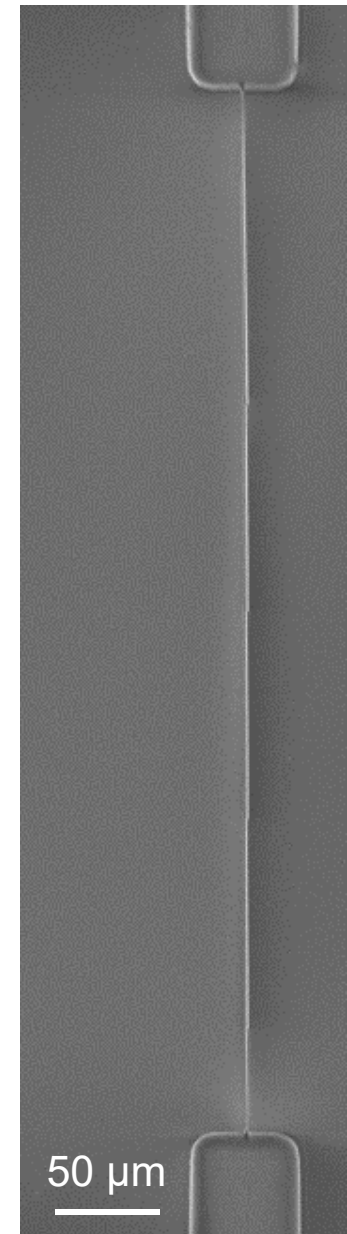
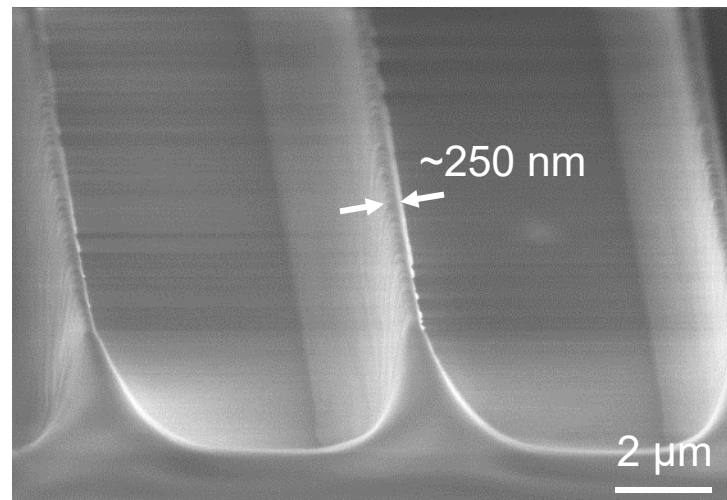
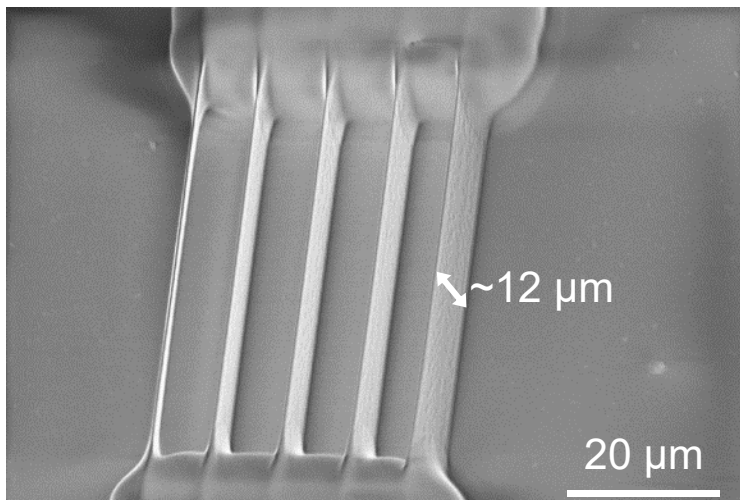
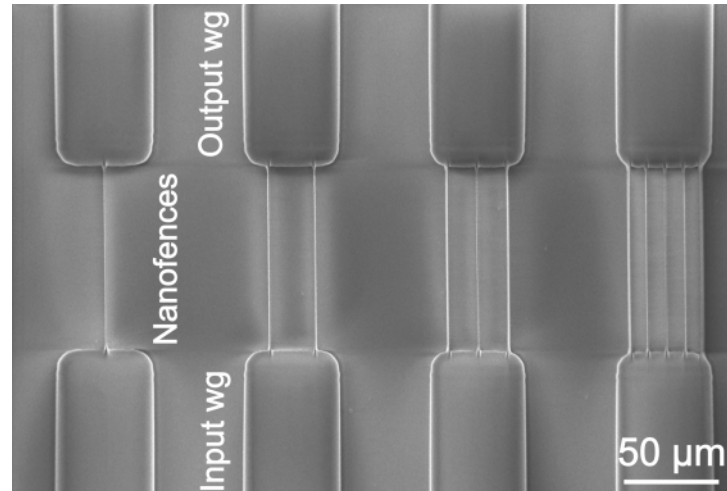


PSI development:
digital pixel particle
camera for
CERN: 48 mega pixel,
40 million images
per second.

Photonic nanofences: Fabrication results

Direct fabrication of structures

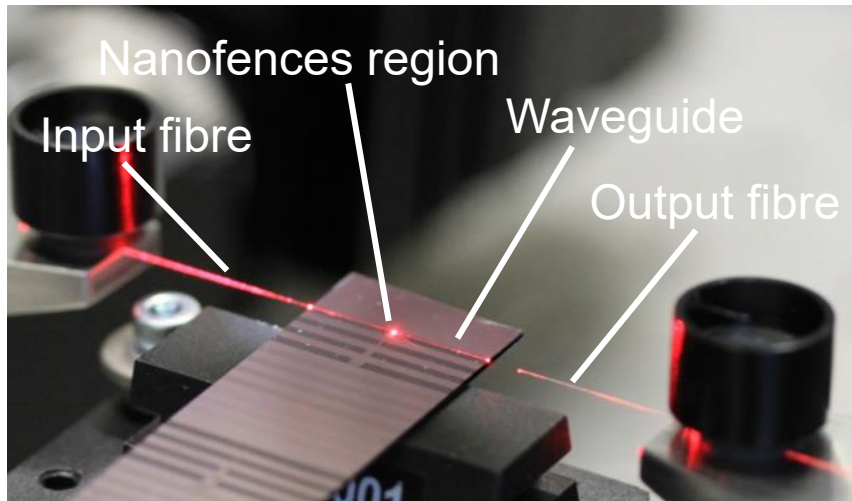
- Fast prototyping
- Smallest structures ~250 nm
- High aspect ratios (> 40:1)
- Structures up to millimeters long
- High design flexibility
- Straightforward combination of micro and nanostructures



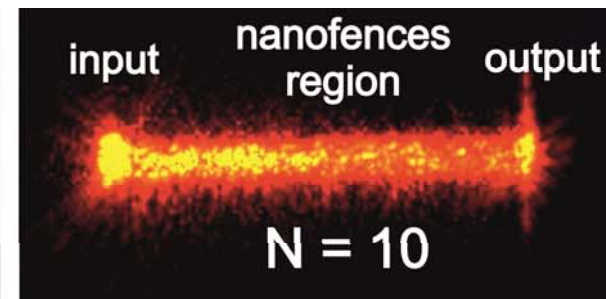
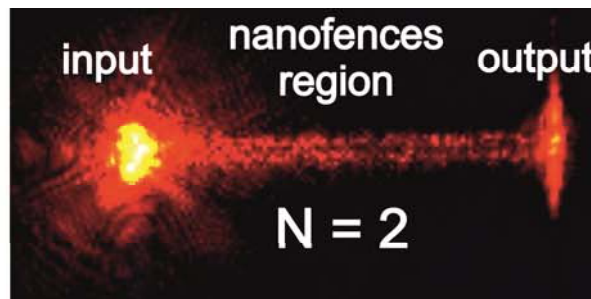
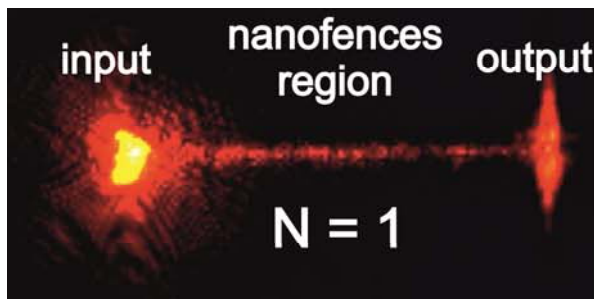
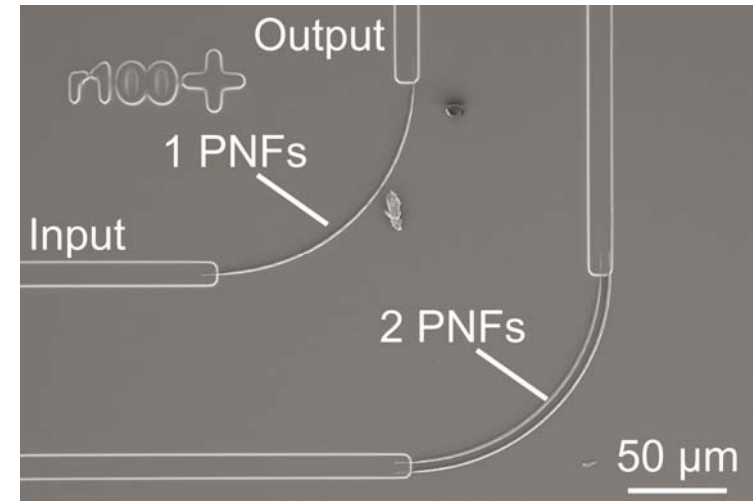
High aspect ratio > 40:1 achieved (5:1 needed)

Photonic Nanofences: Coupling and guiding light

Direct coupling of light



Bent PNFs



Efficient direct coupling of light from standard waveguides to photonic nanofences
Propagation losses in the range of semiconductor photonic nanowires

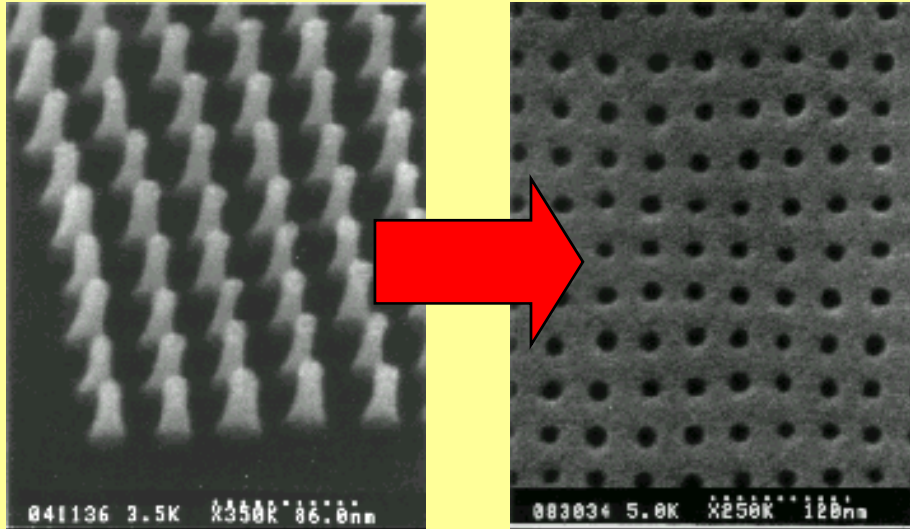
V.J. Cadarso et al. TBP, ACS Nano 2015

Outline

- Nanoimprint in the context of advances in mechanical engineering
- NIL is a **N**ext **G**eneration **L**ithography – true, but not only!
- Is NIL More Moore or More than Moore?
- Non-IC applications, more than Moore – front runners
- What a researcher can contribute
- ... and **More NIL** to come

Nanoimprint and Nanomolding by Mechanical Identification

Nanoimprint Lithography

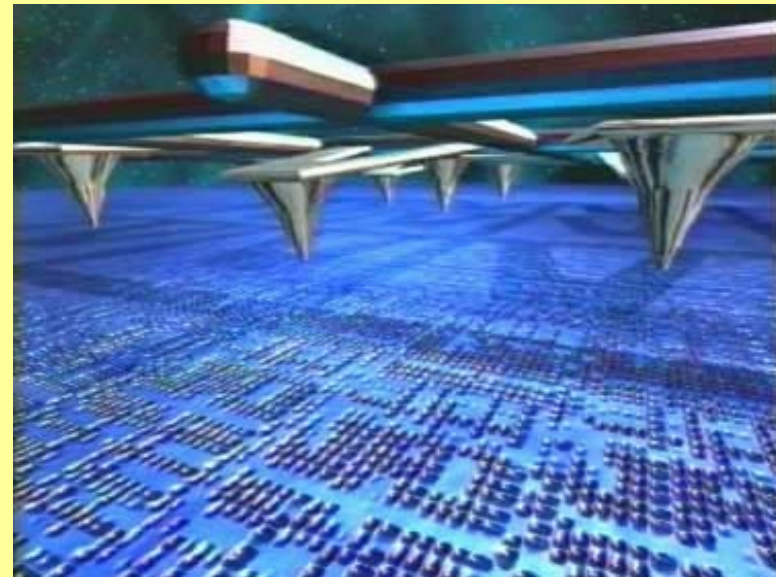


Molding of resist by thermal imprint.
The viscous polymer assumes the shape of the stamp by squeezed flow.

S.Y. Chou, P. R. Krauss and P. J. Renstrom, *Appl. Phys. Lett.* **67**(21), 3114 (1995).

P.R. Krauss and S.Y. Chou, *Appl. Phys. Lett.* **71**(21), 3174 (1997).

Scanning Probe Indentation



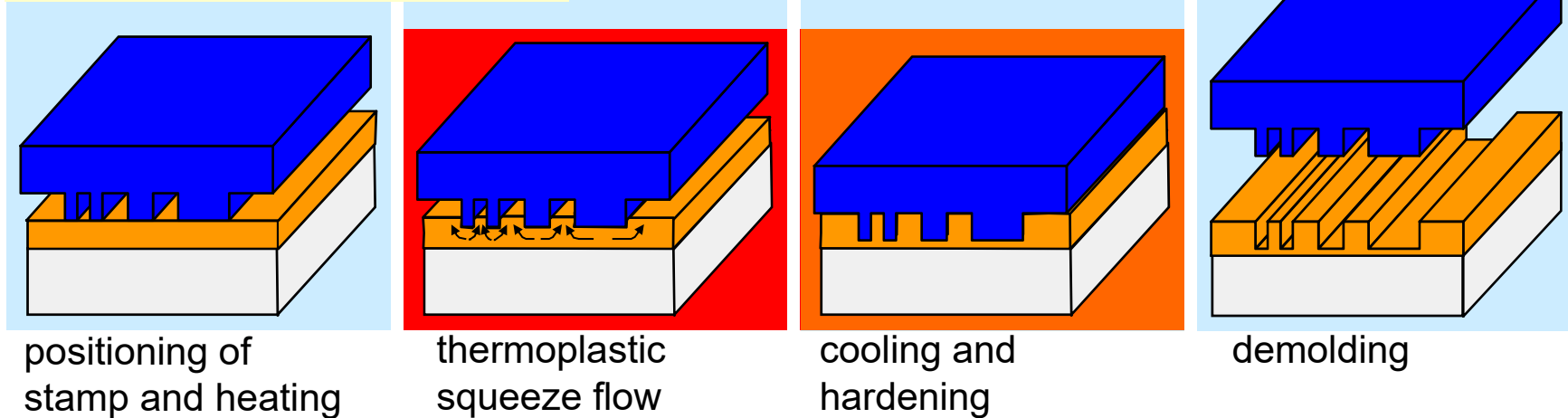
Indentations are generated using an array of heatable SPM tips.

H. J. Mamin and D. Rugar, *Appl. Phys. Lett.* **61**, 1003 (1992)

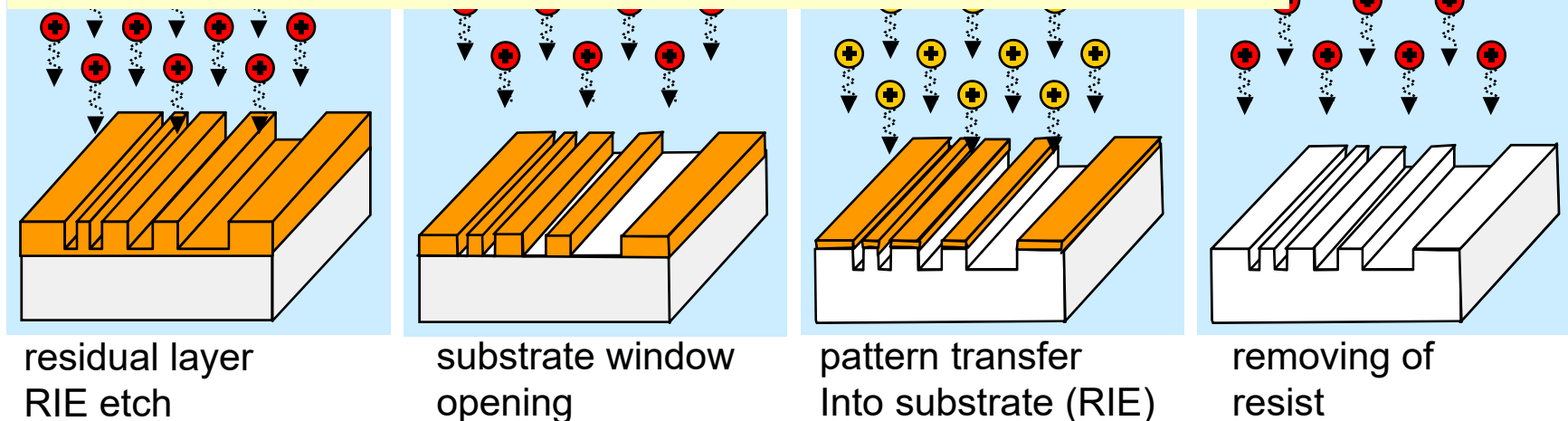
P. Vettiger et al. *Microelectr. Eng.*, **46** (1-4) 101 (1999)

Thermal-NIL + Window Opening + Pattern Transfer

Replica molding (imprint)

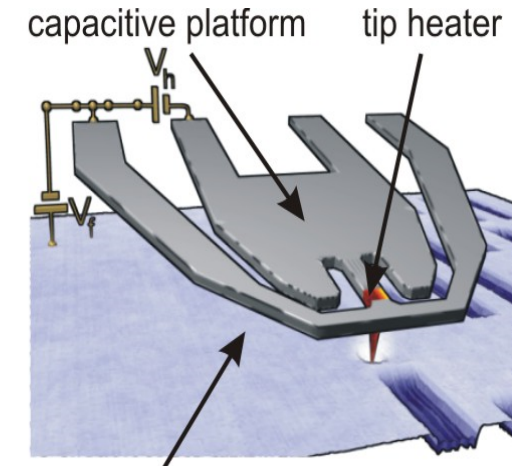
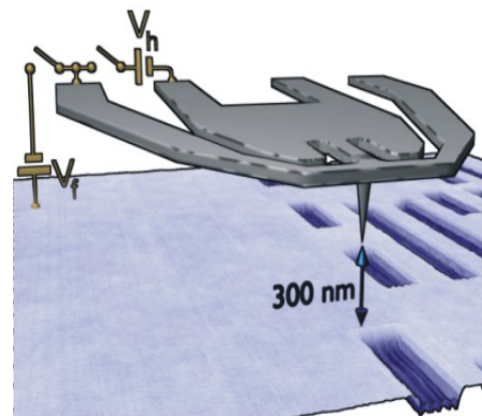
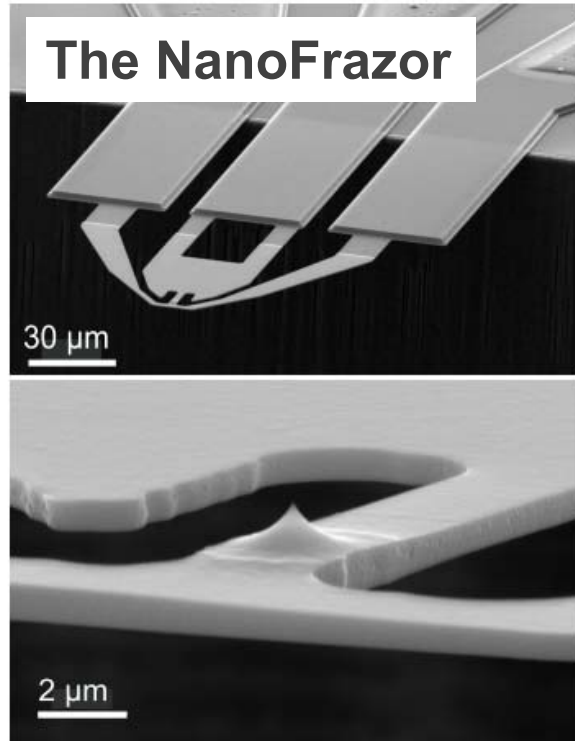


Pattern Transfer (residual layer etch AND substrate etching)



Serial lithography with thermal cantilevers

The NanoFrazor



Thermal sensor for measuring
topography in special AFM imaging mode



Heating of the tip:

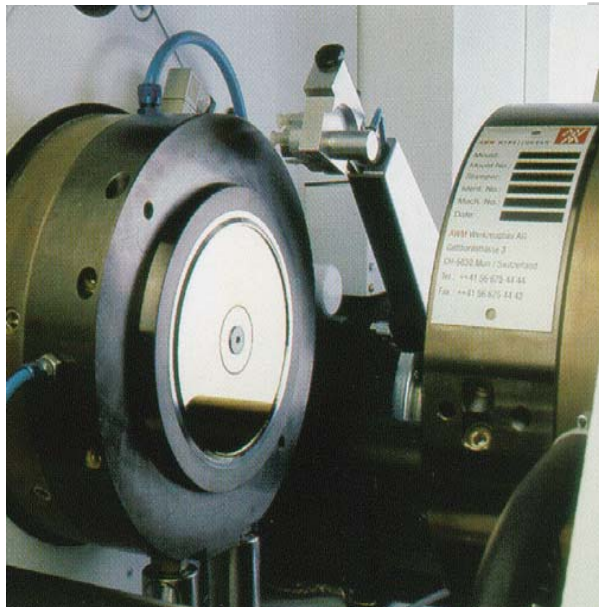
Microheater: $2 \times 2 \mu\text{m}^2$ area with higher electric resistivity
(lower dopant concentration in Si) heats up to 1000°C

Replication Technology – the BIG Advantages of Molding

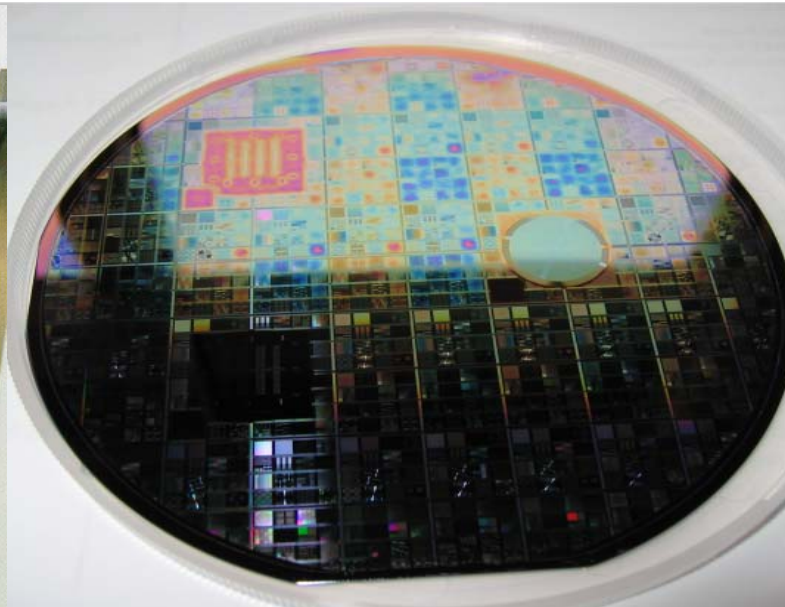
- Freedom of materials: polymer as template
- **3D patterning: molding of complex shapes**
- Small and big structures in one step
- + Working stamp fabrication by replication
- + Hybrid manufacturing schemes



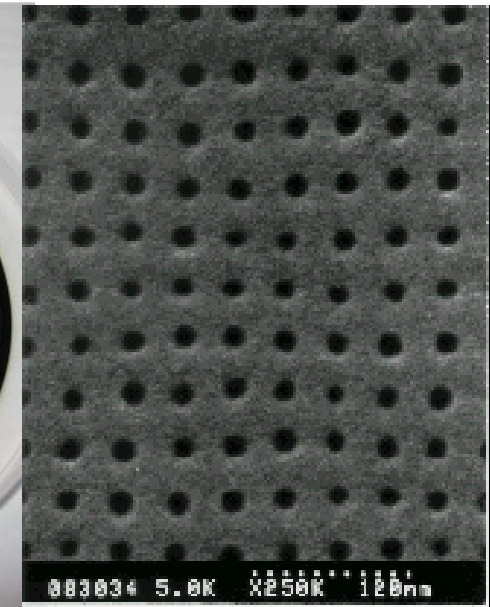
Low-cost



Throughput



Parallel



Resolution

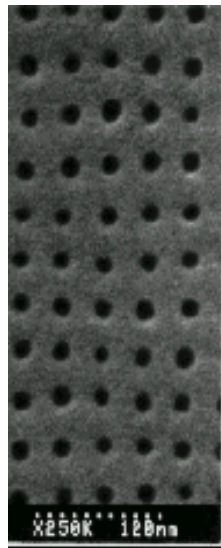
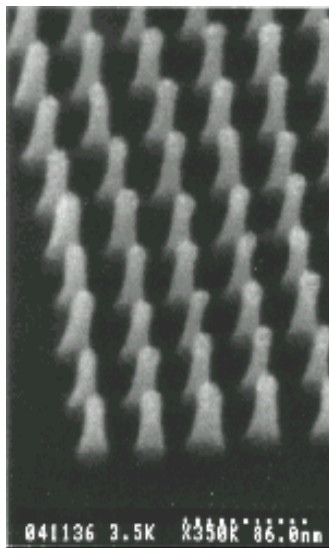
Outline

- Nanoimprint in the context of advances in mechanical engineering
- NIL is a **Next Generation Lithography** – true, but not only!
- Is NIL More Moore or More than Moore?
- Non-IC applications, more than Moore – front runners
- What a researcher can contribute
- ... and **More NIL** to come

What is the Unique Selling Point (USP) of NIL?

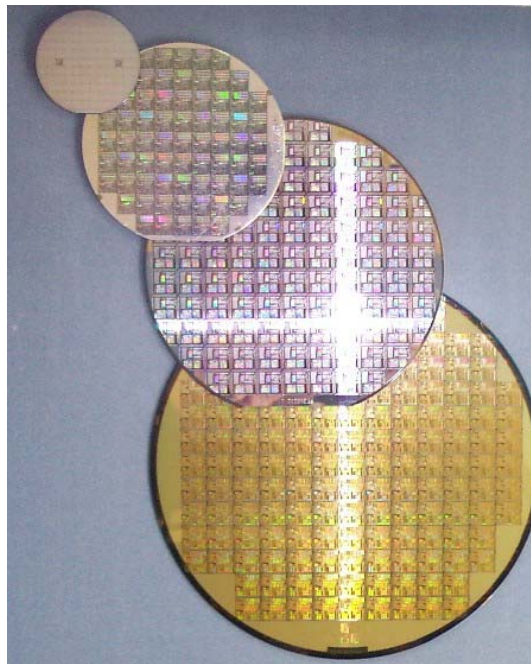
Resolution

no physical limit
→ <10 nm demonstrated



Large area

Scalable
→ large stamps / S&R
(Polymer/Mineral)



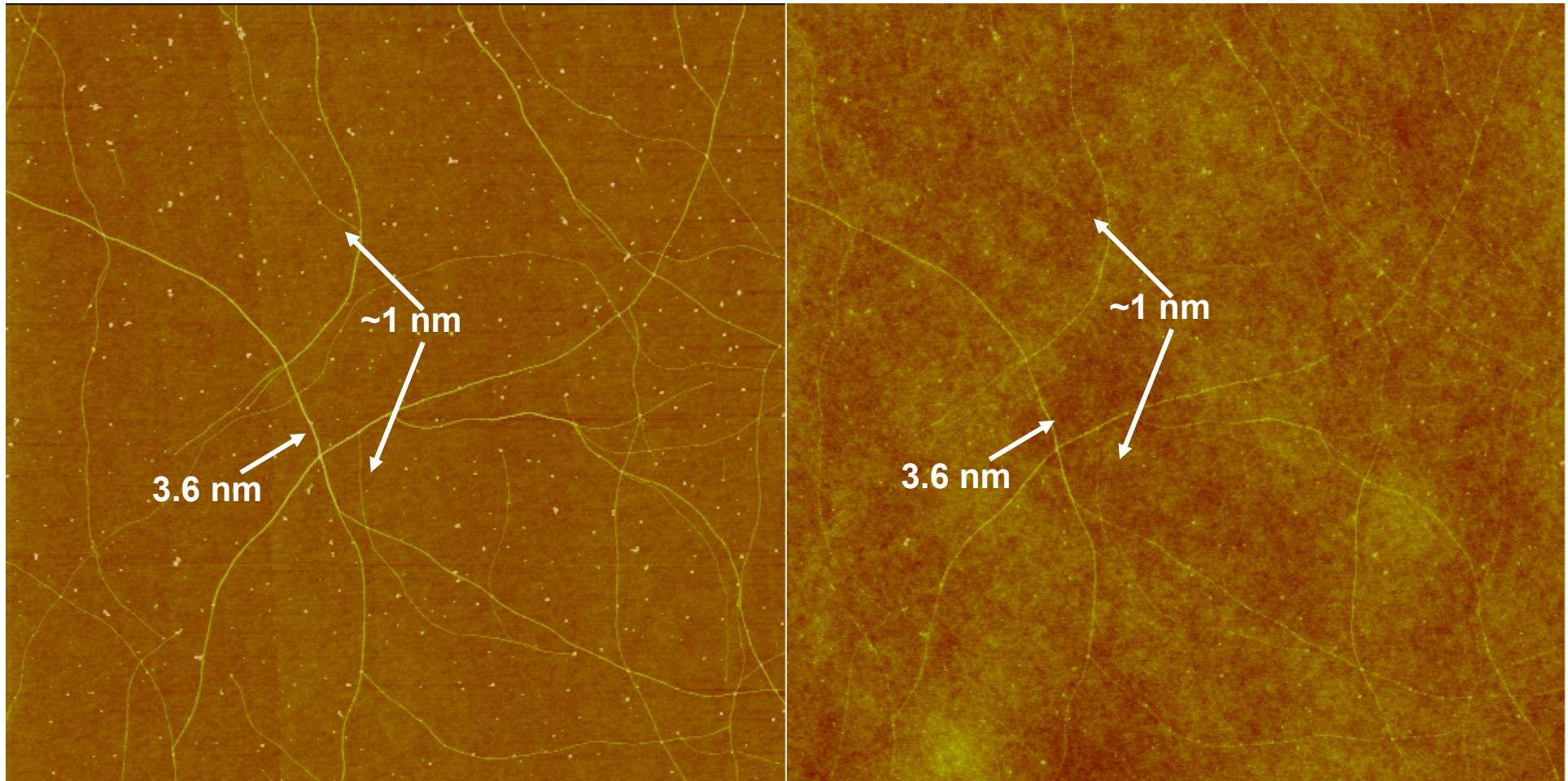
Cost / availability

Simple tools / materials
→ standardization



Note: This has to be proved for applications –
against competing (lithography) processes

Polymer Imprint Lithography With Molecular Scale Resolution

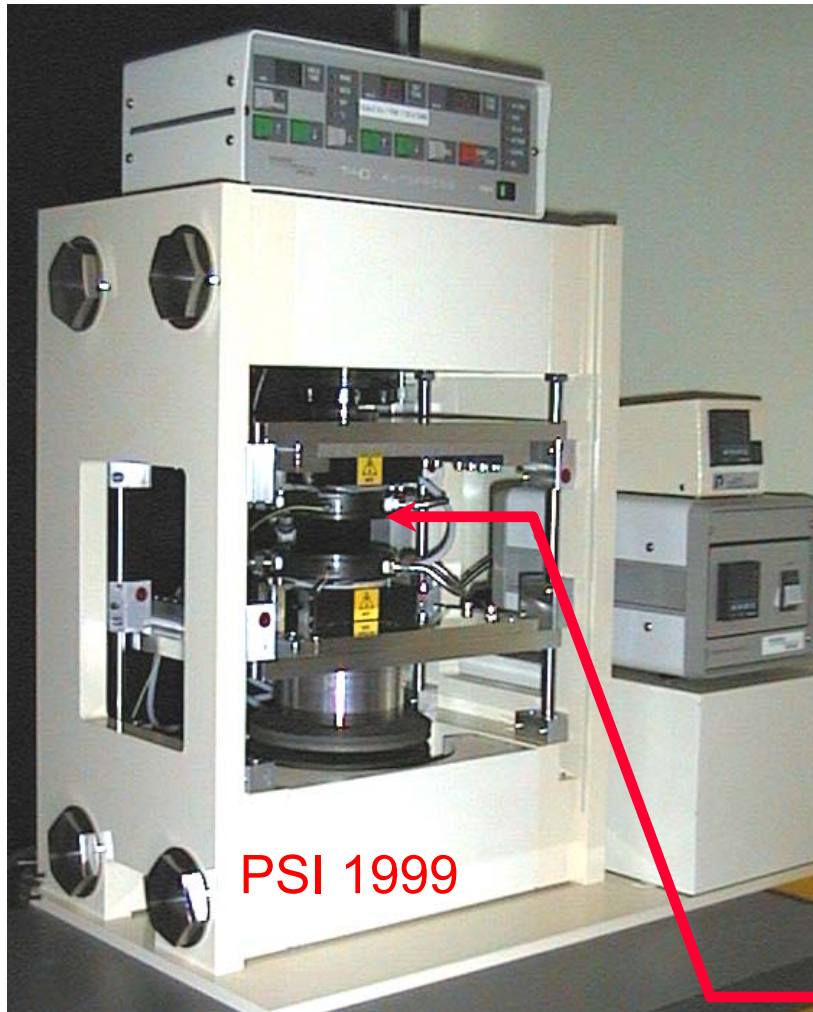


**Master, 10x10 μm
with single nanotubes**

Polymer Imprint, 10x10 μm

IEEE Trans. Nanotechn. **5**, 301 (2006).

Hot Embossing Equipment (in PSI)



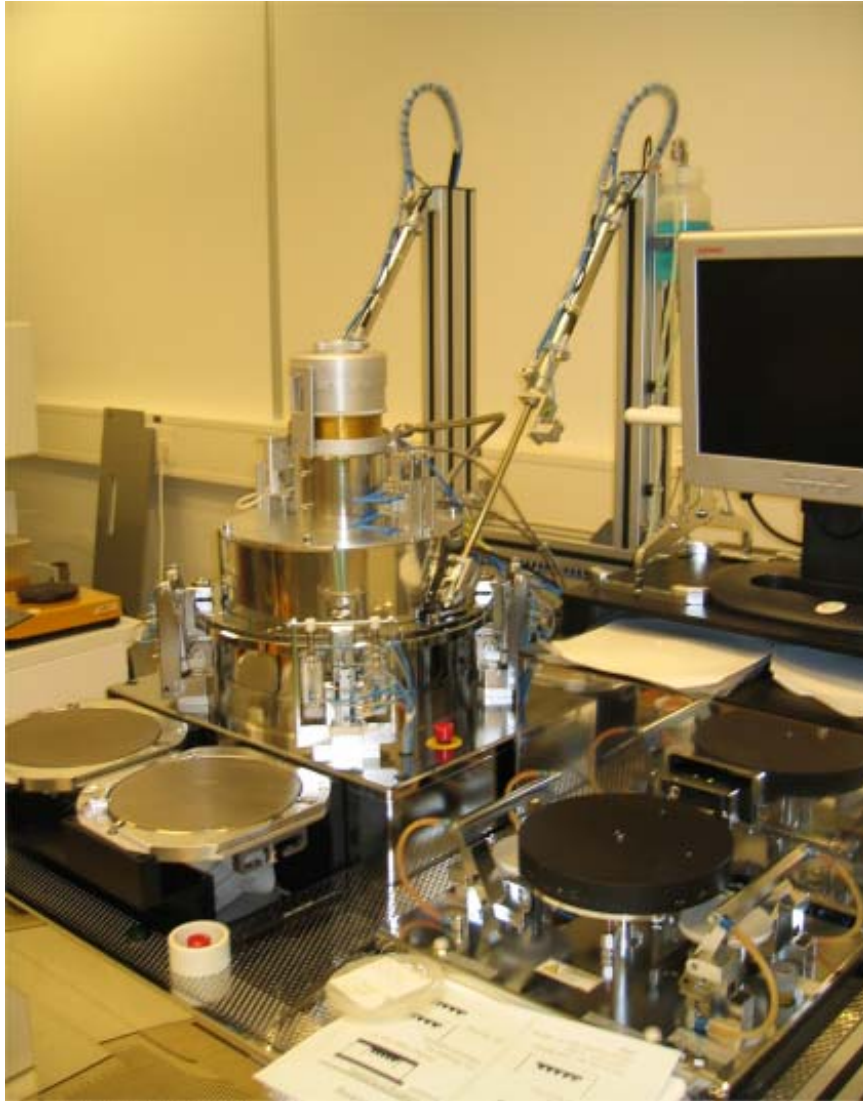
embossing press from Specac

hydraulic press for nanolithography machine parameters:

- **press** : hydraulic (oil)
- **lateral resolution** : < 50 μm
- **stamp** : 15 x 15 mm², up to 100 mm
wafers, substrate silicon
spincoated PMMA (thermoplast)
- **samples** : up to 100 mm wafers
- **temperature** : up to 280 °C
- **applied force** : up to 40 kN
- **conditions** : ambient,
laminar flow (clean room)
- **heating** : electrical
- **cooling** : water / air
- **control** : automatic

process area for sample
and mold insert

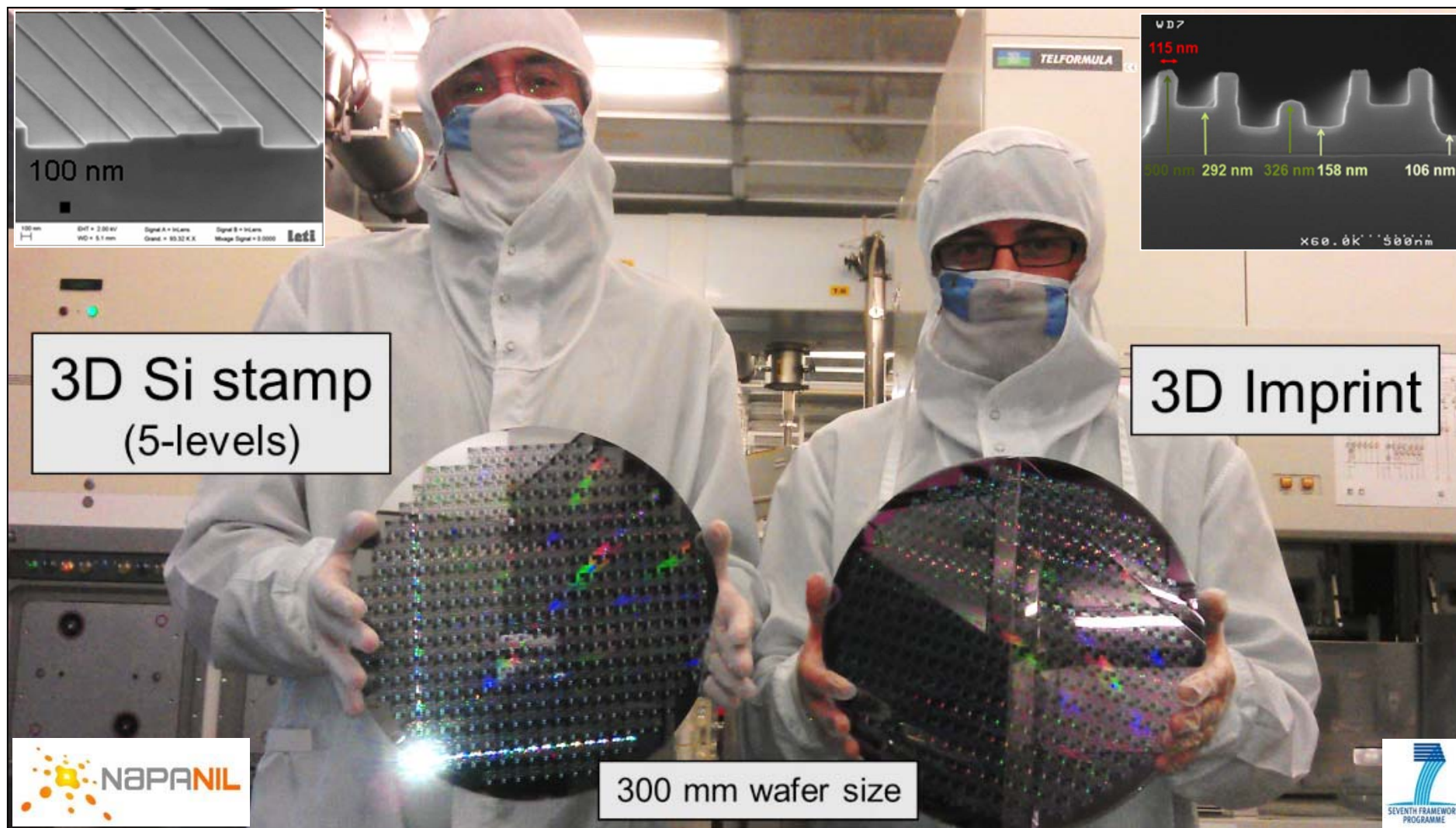
Nanoimprint Machines from EVG 620



8" imprint bonder in LETI / Grénoble

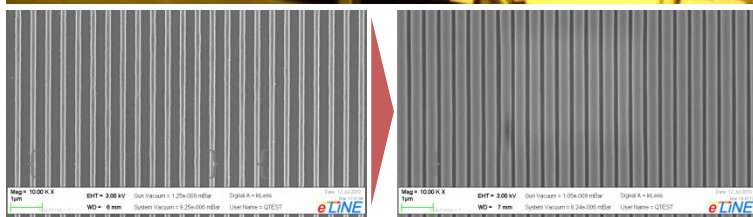
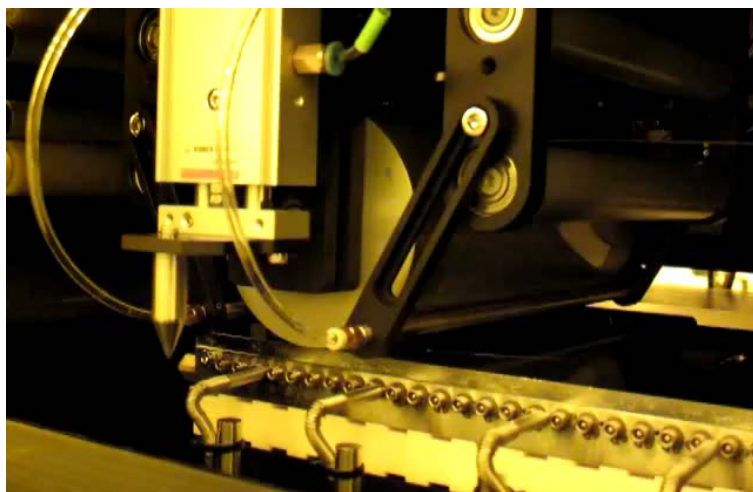
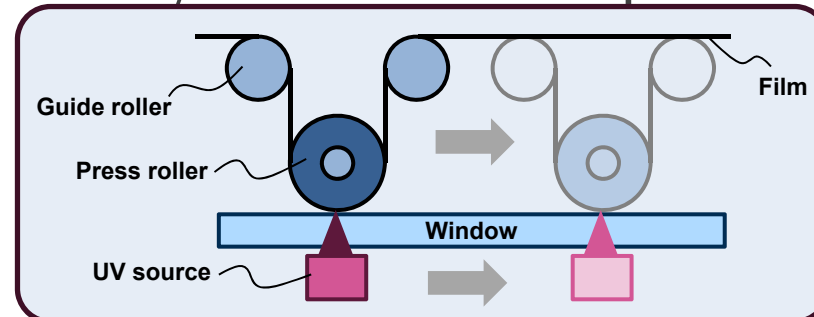
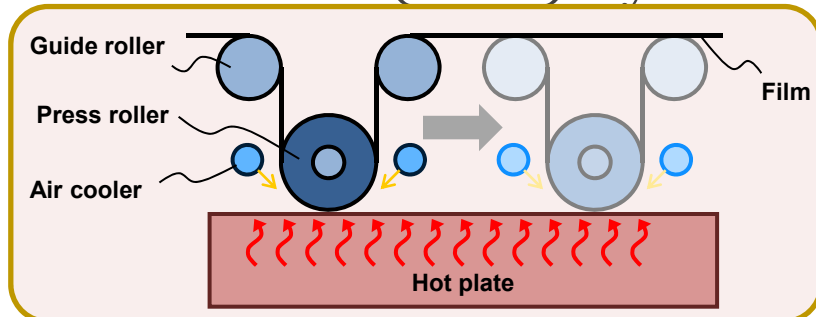
- imprint under vacuum
 - alignment separately in mask aligner
- (+) good accessibility, usable for anodic bonding
- (-) low pressure, speed (no water cooling)

Large Area 3D Imprint Capabilities (Plate-to-Plate)



With courtesy of Stéfan Landis & Vincent Reboud (LETI-CEA, France)

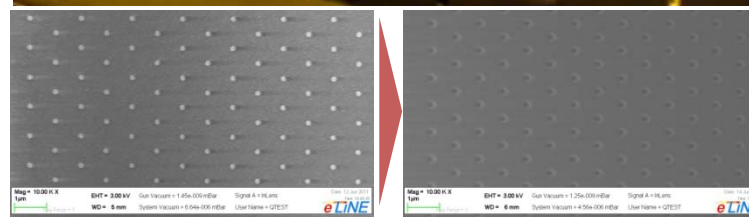
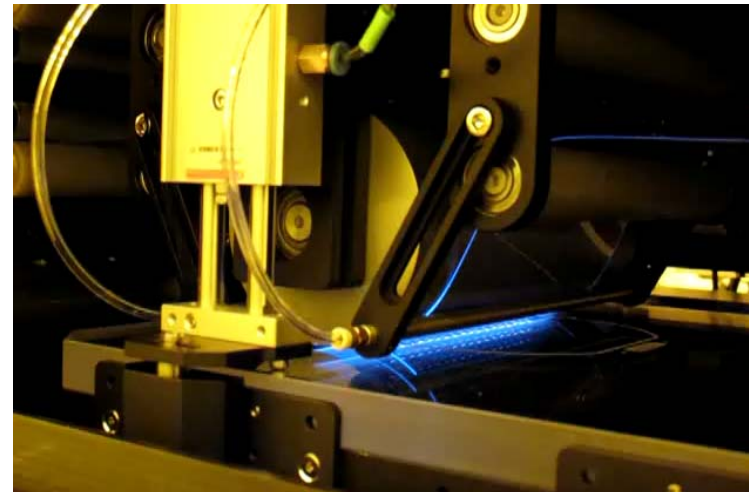
Roll-to-Roll (R2R) System: Thermal/UV-assisted Imprint



180 nm-width and 470 nm-pitch
line pattern on a Si stamp

Transferred pattern on a PC
film by the thermal-RNIL system

Thermal-RNIL Mode



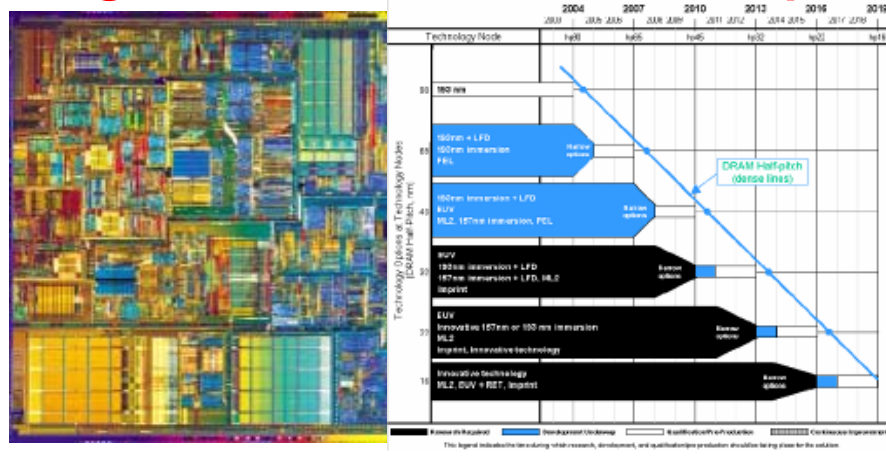
140 nm-diameter and 1 μ m-pitch
dot array on a PUA/glass stamp

Transferred pattern on a PC
film by the UV-RNIL system

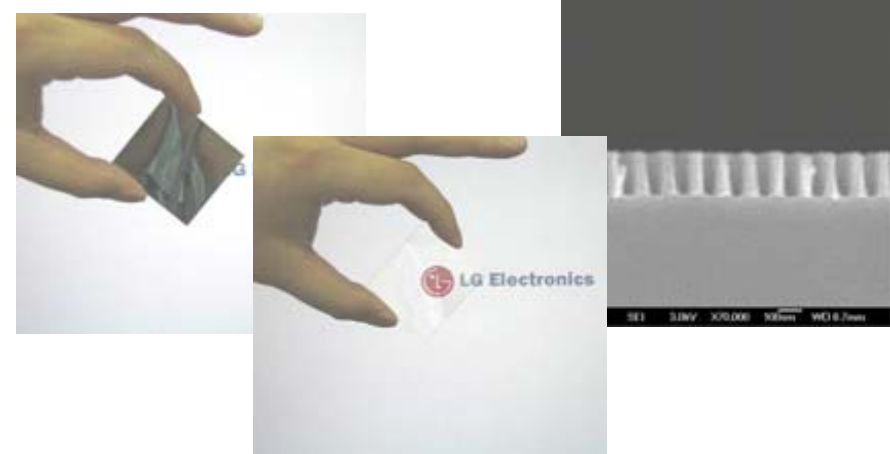
UV-RNIL Mode

Nanopatterning – Main NIL Applications

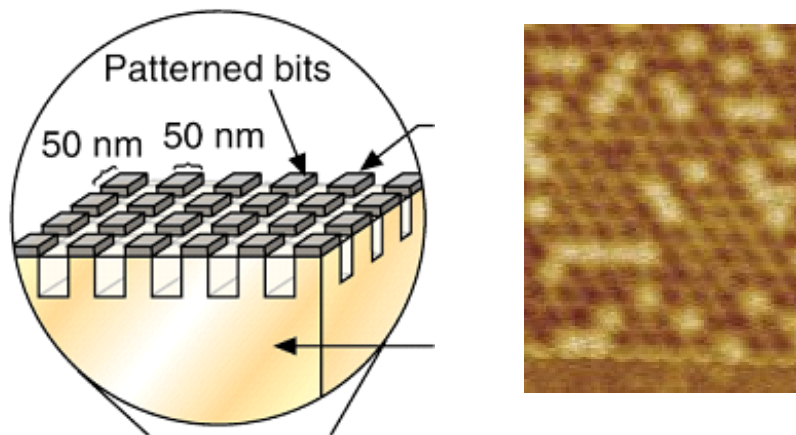
High End Microelectronic Chips



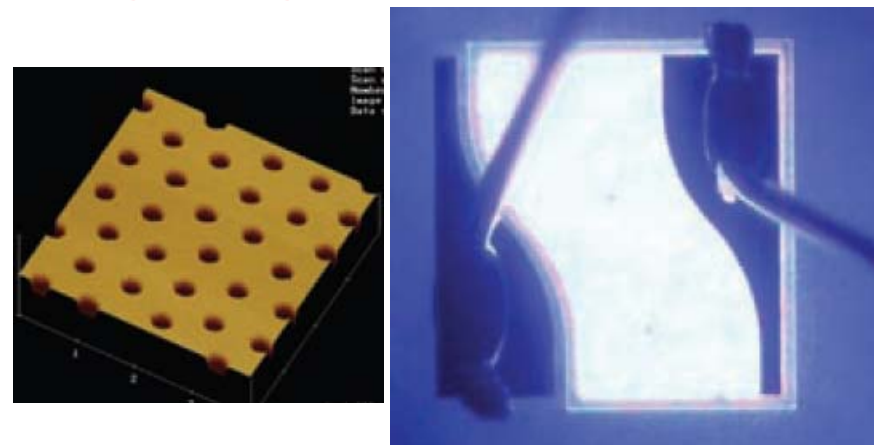
Wire Grid Polarizer



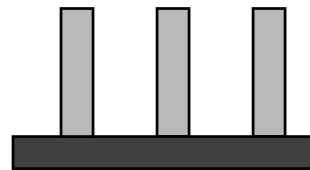
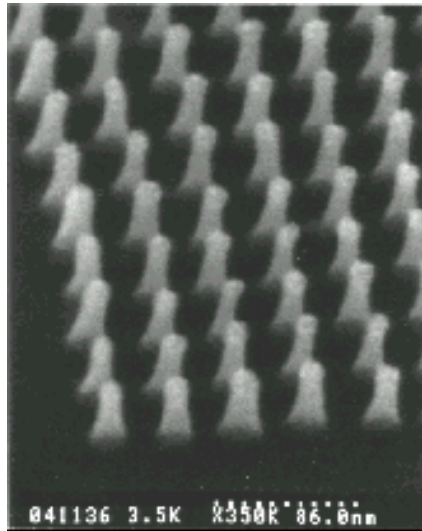
Patterned Magnetic Media



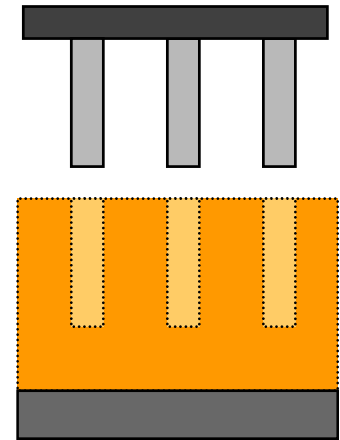
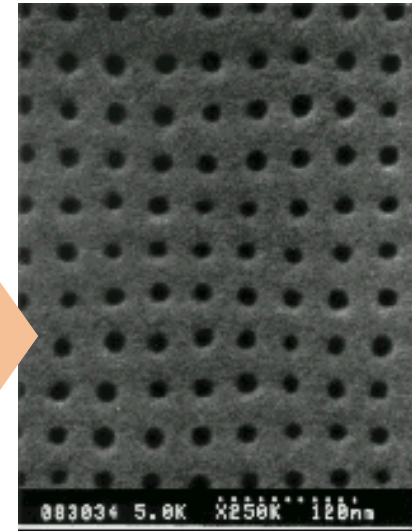
High Brightness LEDs



Fabrication of Nanodots in Metal



**Hot Embossing
Lithography**



**master:
embossing stamp**

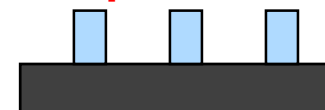
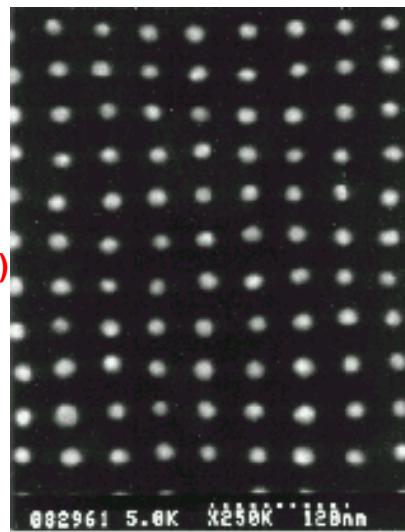
- fabrication with e-beam exposure and RIE
- material: Si or SiO₂ (not specified)
- size: down to 10 nm
- period: 40 nm
- depth: 60 nm

molded structure
- material: PMMA
on Si

Lift-off

metal dots

- material: not specified
- excellent uniformity over 1 square inch

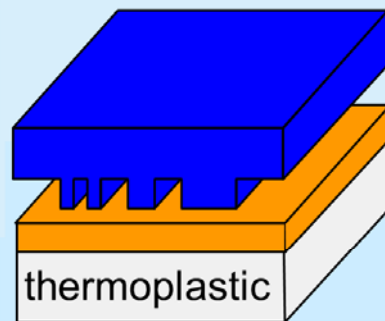


Source: S. Chou, NSL, 1998

Replication (thermal, UV-, step&repeat and roll-to-roll NIL)

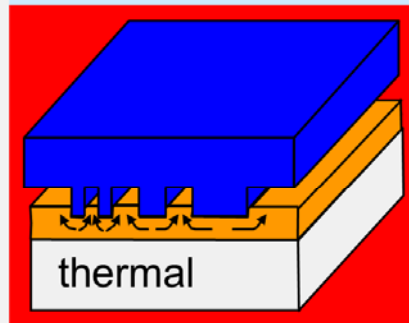
Stamp alignment

on resist coated
substrate
spin-coated film
or dispensed droplets



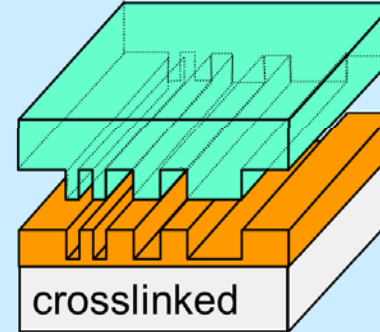
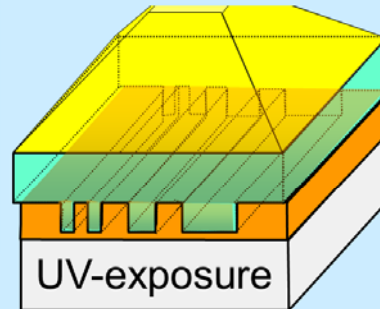
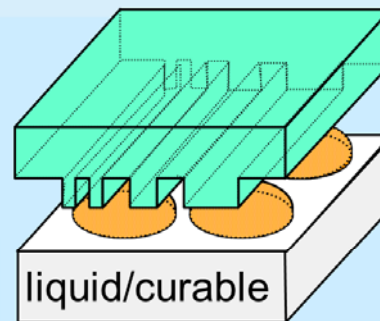
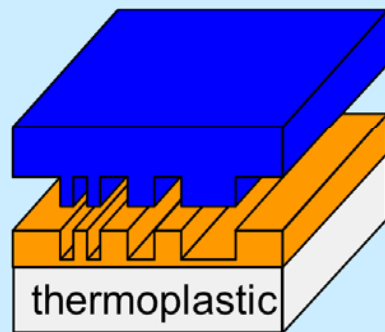
Thermal or UV-light assisted nanoimprint

viscous squeeze and
capillary induced flow

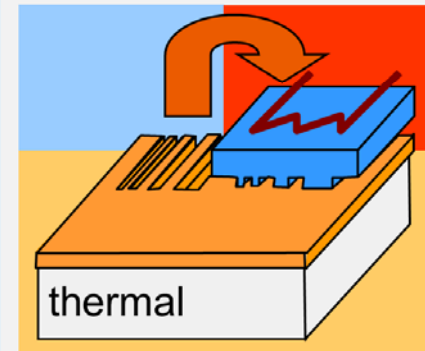


Demolding

stamp detachment
from molded resist
(thickness contrast)
and re-use

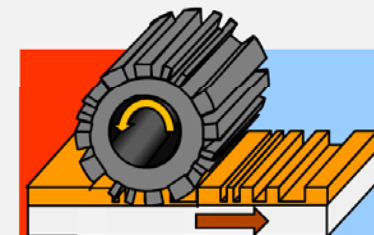


Lateral area enhancement by step&repeat



Roller imprint

roll-to-rolle / roll-to-plate

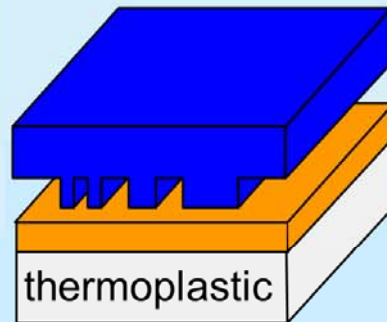


thermal

Replication (thermal, UV-, step&repeat and roll-to-roll NIL)

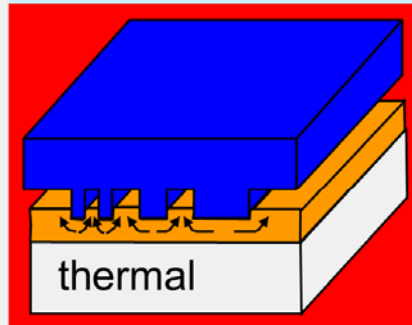
Stamp alignment

on resist coated substrate
spin-coated film
or dispensed droplets



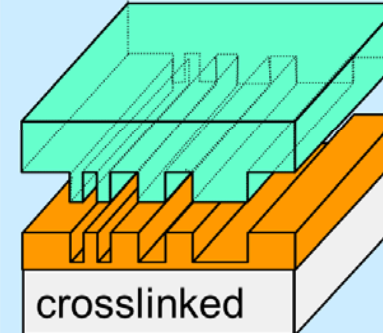
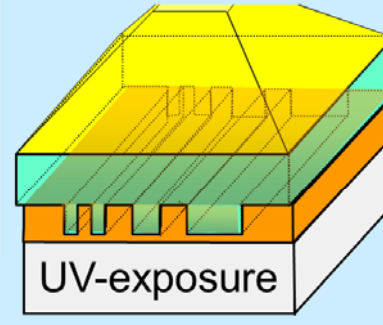
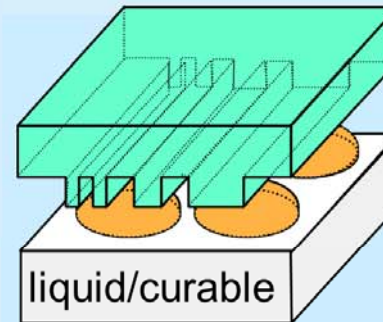
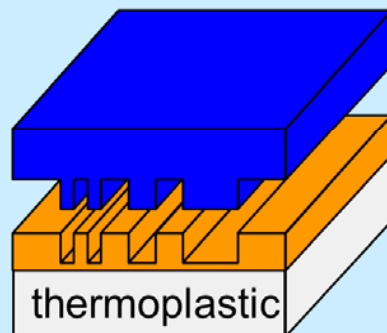
Thermal or UV-light assisted nanoimprint

viscous squeeze and capillary induced flow

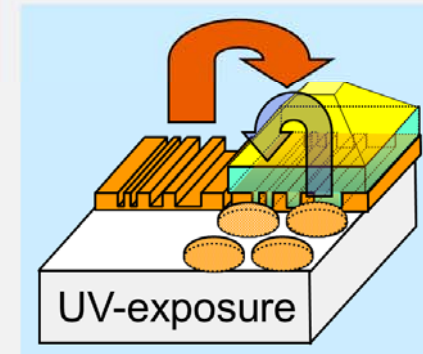


Demolding

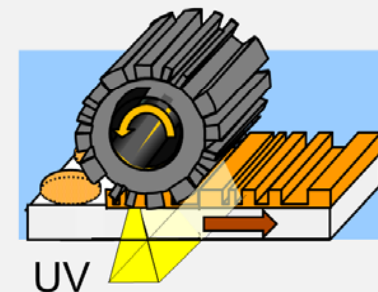
stamp detachment
from molded resist
(thickness contrast)
and re-use



Lateral area enhancement by step&repeat



Roller imprint roll-to-roll / roll-to-plate



Pattern transfer (window opening and substrate patterning)

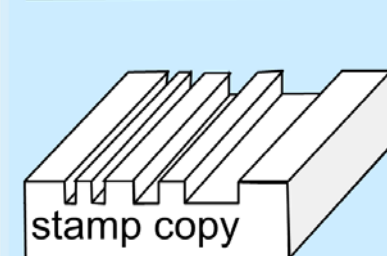
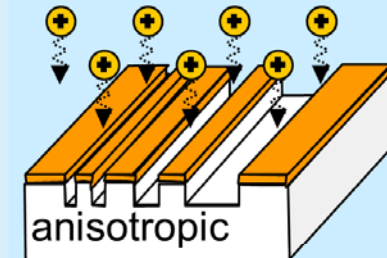
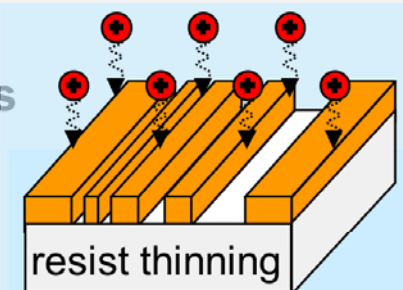
Pattern transfer for opening of substrate windows
residual layer etch

Pattern transfer into substrate

- etching (RIE, wet)
- lift-off
- electroplating

Patterned substrate

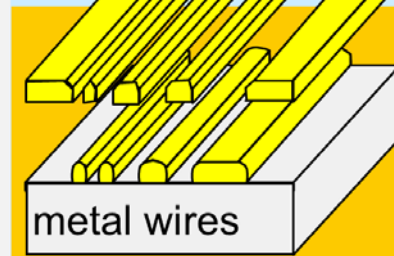
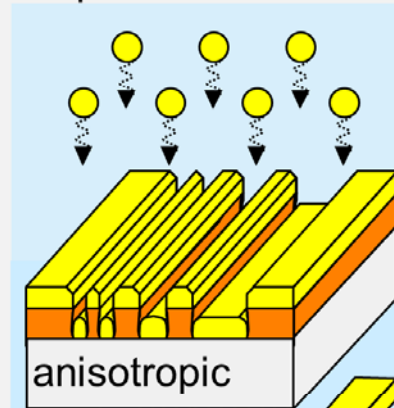
Subtractive: etching



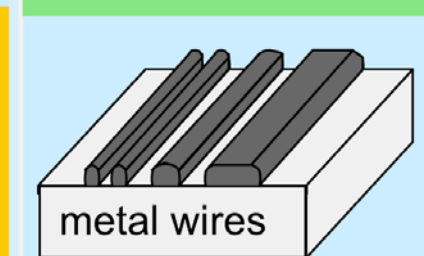
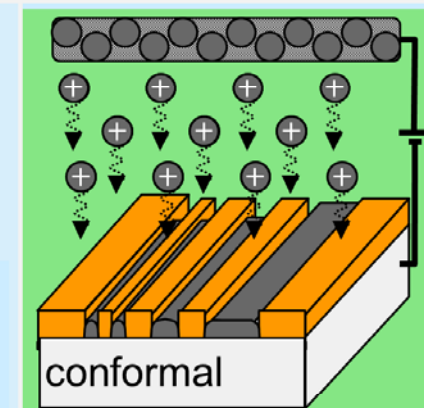
Additive: templated deposition

lift-off

selective removal of deposited material



electroplating
from seed layer



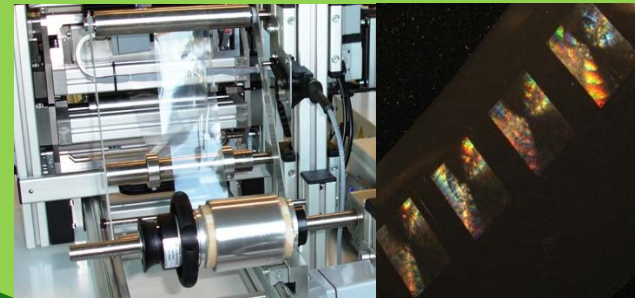
NOTE: Only pattern transfer makes NIL a true «lithography»

Replication toolbox

Thermal / UV nanoimprint



Roll-to-roll thermal imprint



Replication technology toolbox

Injection molding



Microthermoforming



NOTE: There are «lithographic pattern transfer» and «direct-use» functional material applications

Outline

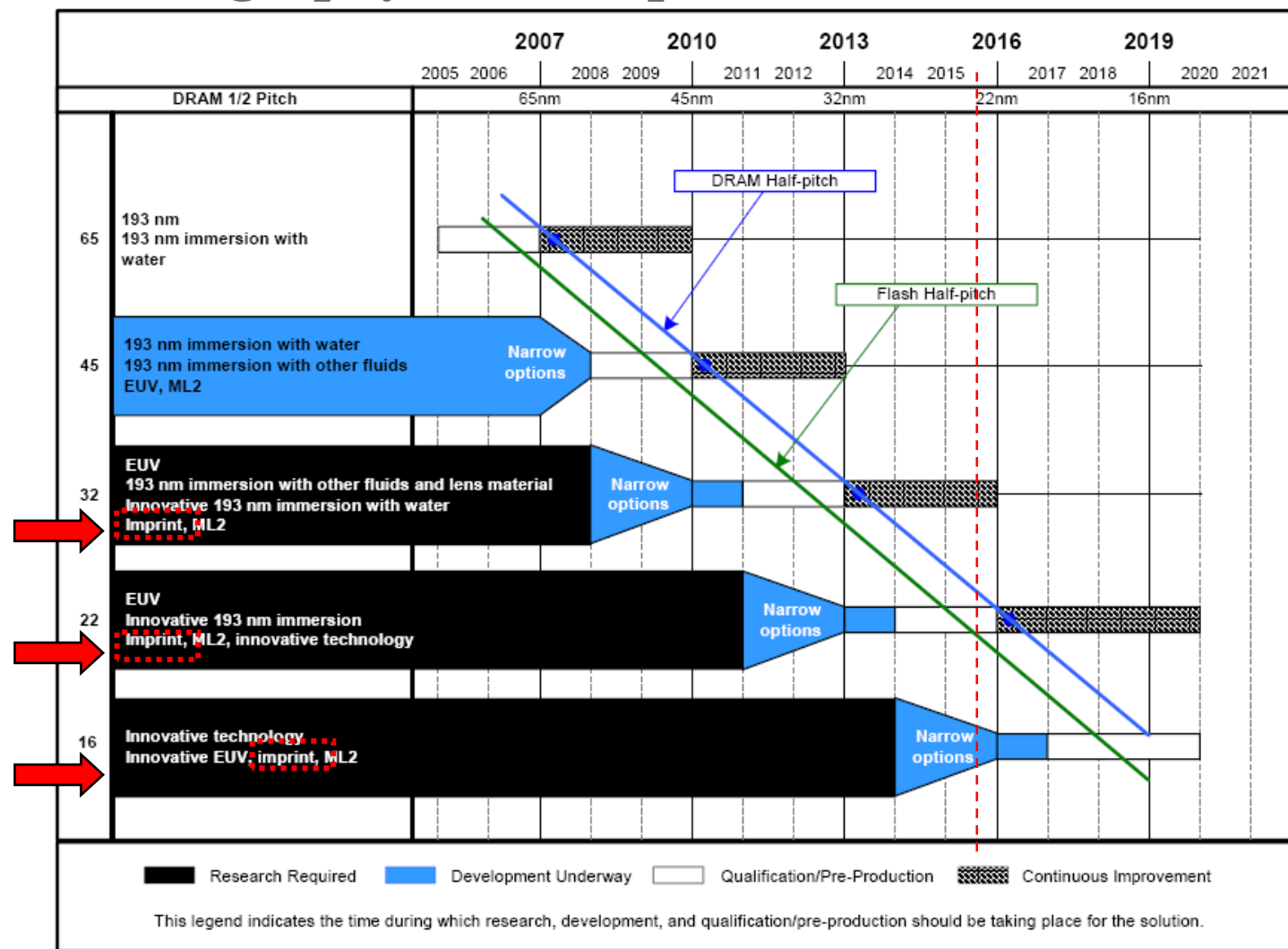
- Nanoimprint in the context of advances in mechanical engineering
- NIL is a **N**ext **G**eneration **L**ithography – true, but not only!
- Is NIL More Moore or More than Moore?
- Non-IC applications, more than Moore – front runners
- What a researcher can contribute
- ... and **More NIL** to come

Moore's law – the 'inner law' of growth for (integrated circuit) microchip manufacturing

Moore's law: roadmap defined 1965 by Gordon Moore (INTEL)
transfer of economic rules into the world of lithography
«The number of transistors has to double every 18 months»

⇒ engineers are forced to do a technological advancement

Lithography Roadmap – Moore's Law



Draft of 2006 update to ITRS

Optical Lithography

through the 45 nm node; and possibly beyond

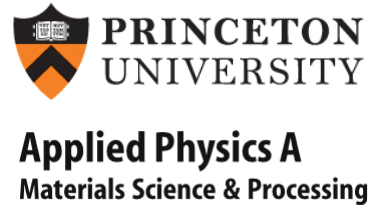
Imprint Lithography

appears on the roadmap as a potential solution at the 32 nm node



Lithography Exposure Tool Potential Solutions

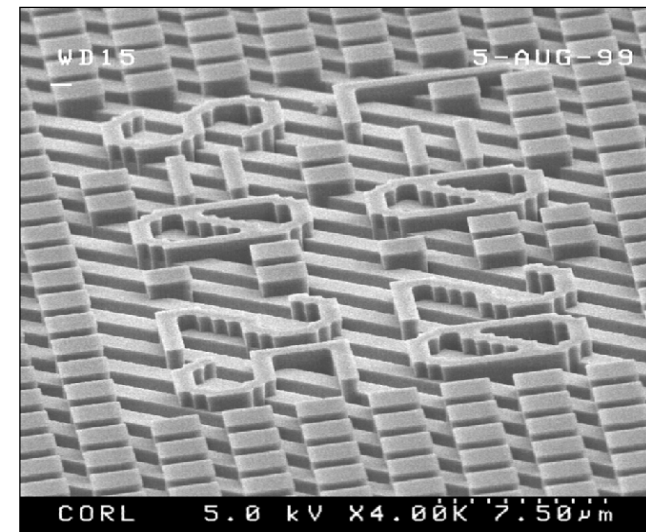
2009-10: Intel announces 32 for 2009 and 22nm for the end of 2011; 14 nm for 2016



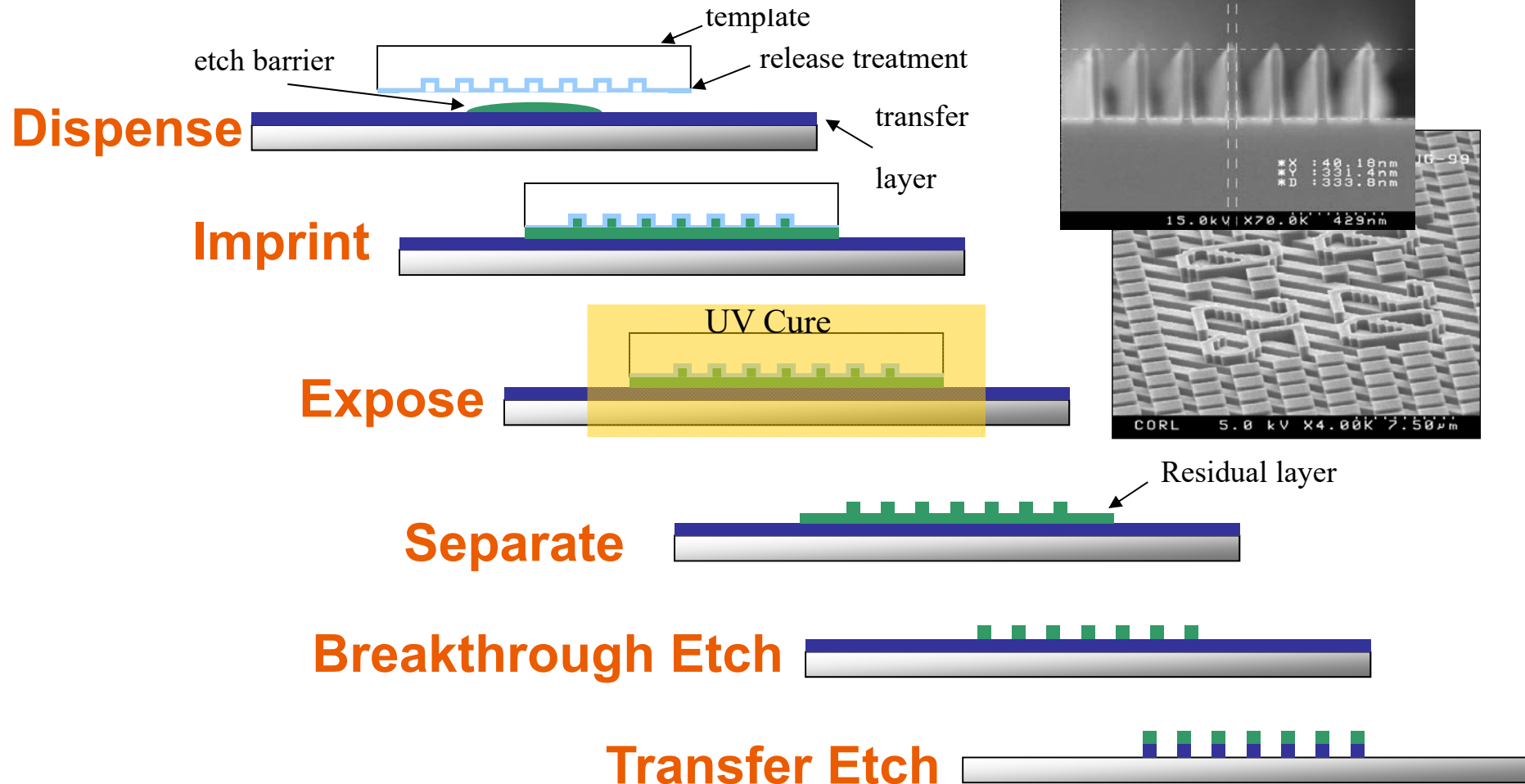
Stephen Y. Chou, Princeton

“MIT’s Technology Review named nanoimprint lithography one of “ten emerging technologies that will change the world”. The magazine wrote in 2003 that “ultimately, nanoimprinting could become the method of choice for cheap and easy fabrication of nano features in such products as optical components for communications and gene chips for diagnostic screening..”

Appl. Phys. A (2015) 121:317–318



Jet and Flash Imprint Lithography (JFIL) Process

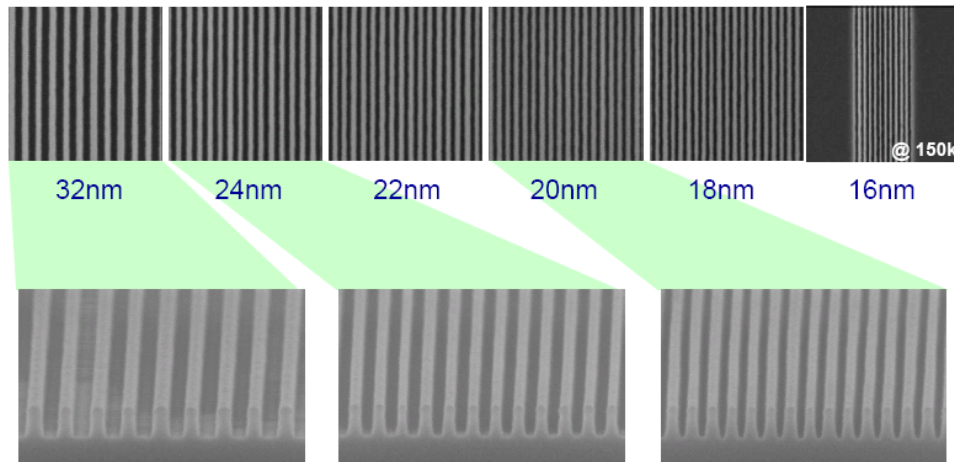


SFIL/JFIL was commercialized by Molecular Imprints Inc (MII)

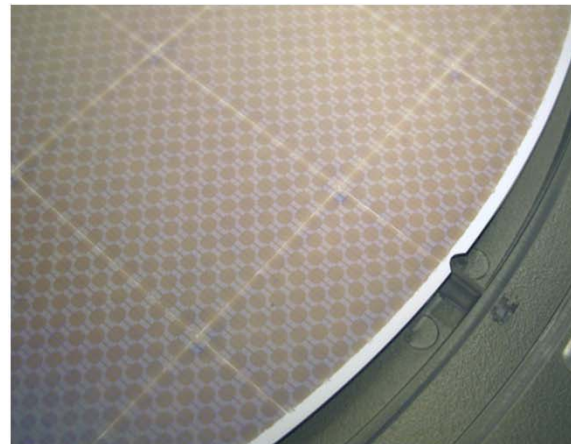
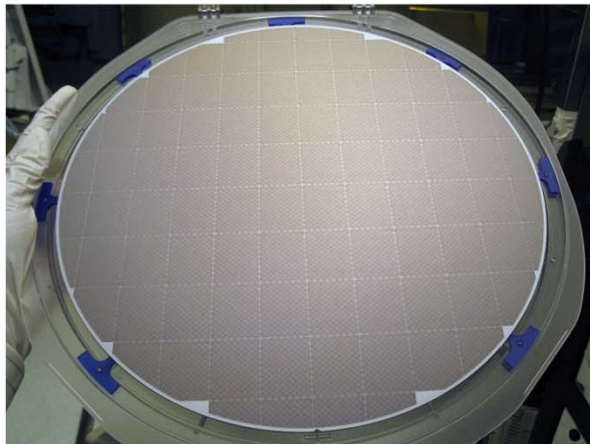
Courtesy Grant Willson, University of Texas at Austin

Canon acquired Molecular Imprints in 2015

Line&Space pattern 1/2Pitch



Etched quartz images



- ⇒ Fast «jetting» of resist
- ⇒ Dust filtering (micro-environment)
- ⇒ Cluster of 4 machines for 60 wafers per hour
- ⇒ Overlay, yield and homogeneity over 300 mm wafers

Courtesy Doug Resnick, Canon Nanotechnology

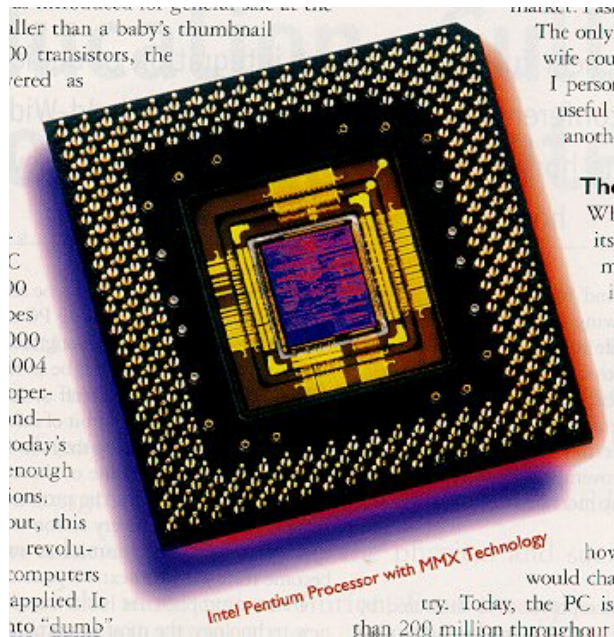
Moore's law – the 'inner law' of growth for (integrated circuit) microchip manufacturing

Moore's law: roadmap defined 1965 by Gordon Moore
transfer of economic rules into the world of lithography
«The number of transistors has to double every 18 months»
⇒ engineers are forced to do a technological advancement

More Moore: NIL as a next generation lithography
«The number of transistors has to double every 18 months»

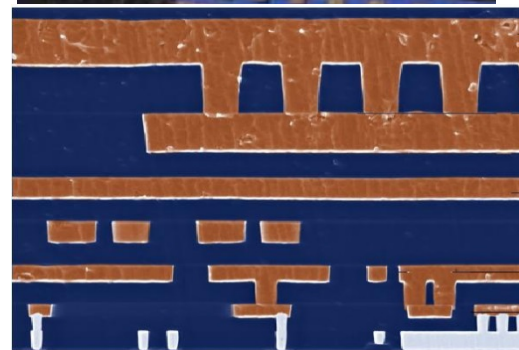
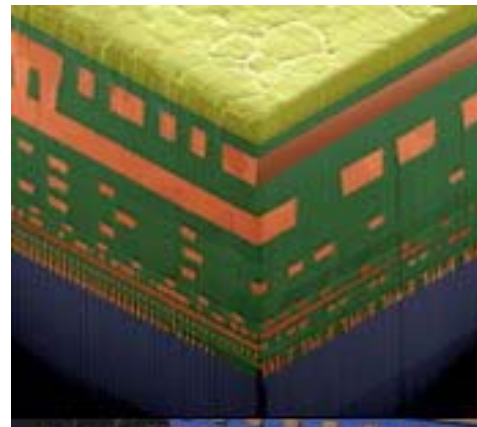
- ⇒ NIL is forced to obey Moore's law (resolution, defectivity)
- ⇒ Different priorities (defectivity), resolution not much smaller than with DUV
- ⇒ NIL has to be cheaper than other high-end lithographies

Integrated Chips – Interconnect Layer

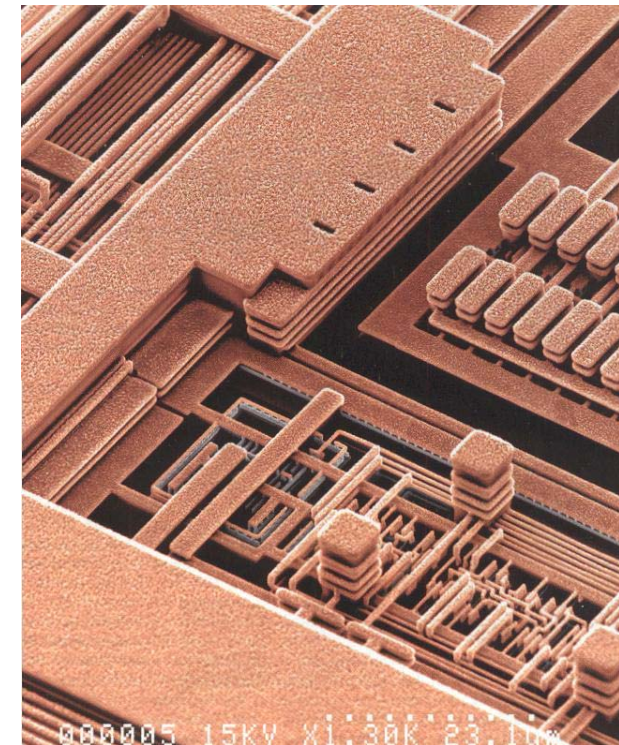


Intel Pentium Processor

Nanoimprint needs to be used for transistors with smaller gate lengths – or for the interconnect layer



IBM copper interconnect with six metal layers (year: 1998)



IBM CMOS 0.12 mm Dual Damascene process

<http://www-03.ibm.com/chips/about/technology/makechip/interconnect/>

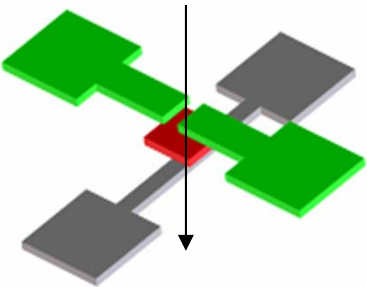
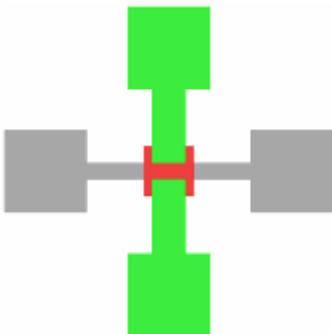
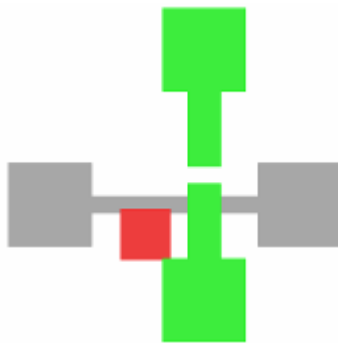
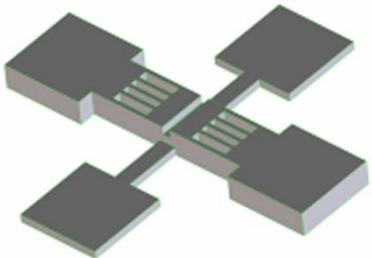
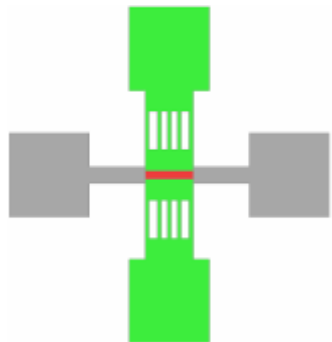
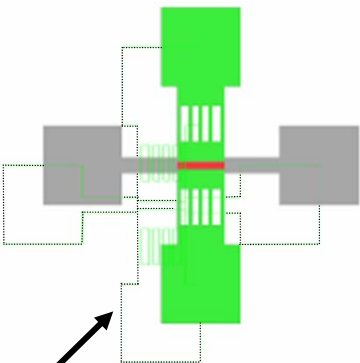
Moore's law – the 'inner law' of growth for (integrated circuit) microchip manufacturing

More than Moore: NIL with multilayer approach (with benefits)
«The number of transistors has to double every 18 months»

⇒ NIL is forced to obey Moore's law (resolution, defectivity)
at a much lower price (cost of ownership)

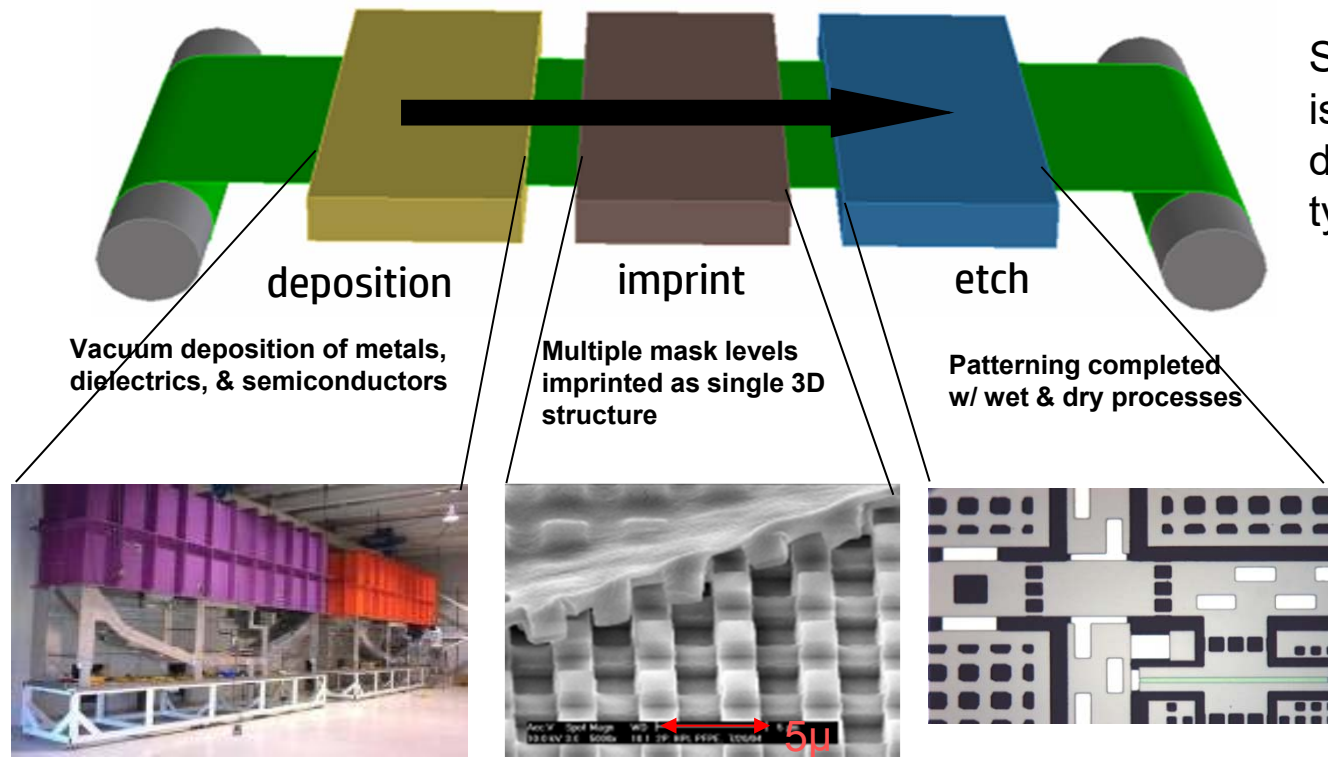
**BUT NIL does not only replace single lithographic steps,
but also has added value
by reducing the number of process steps**

SAIL: Self-Aligned Imprint Lithography

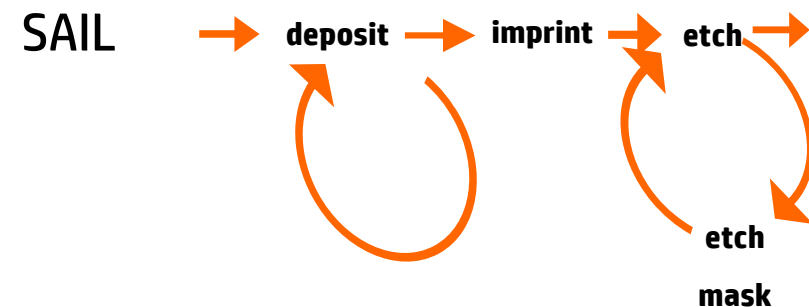
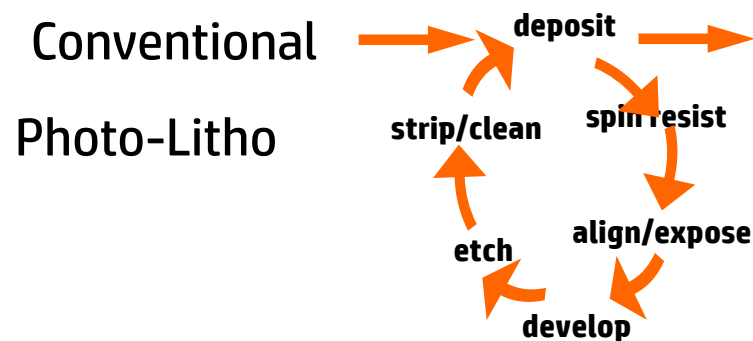
Photolithography	 <p>Multiple masking and alignment steps required</p>	 <p>Different mask used to pattern each layer</p>	 <p>Process distortion of 200ppm results in 20μ misalignment over 10cm</p>
SAIL	 <p>SAIL encodes multiple patterns and alignments into thickness modulations of a monolithic masking structure</p>	 <p>Single mask used to pattern all the layers multiple times</p>	 <p>No misalignment because mask distorts with substrate</p>

Carl Taussig, HP Labs

SAIL: Self-Aligned Imprint Lithography



SAIL Process flow is radically different from typical thin film



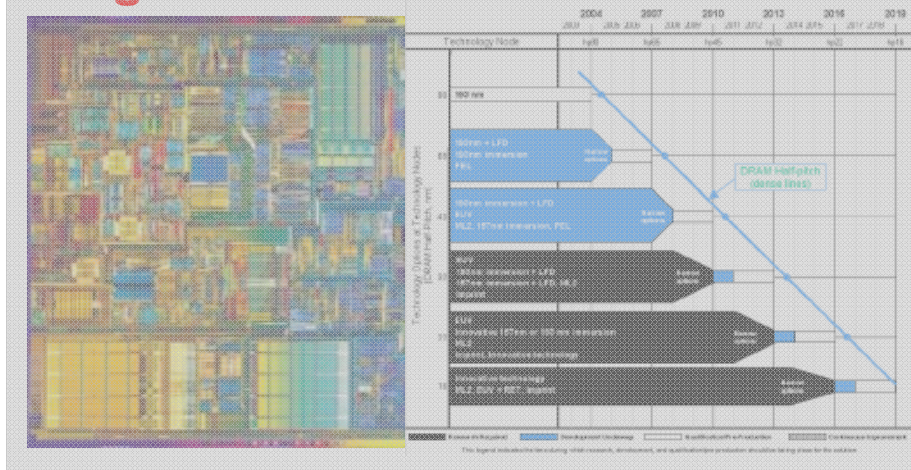
Carl Taussig, HP Labs

Outline

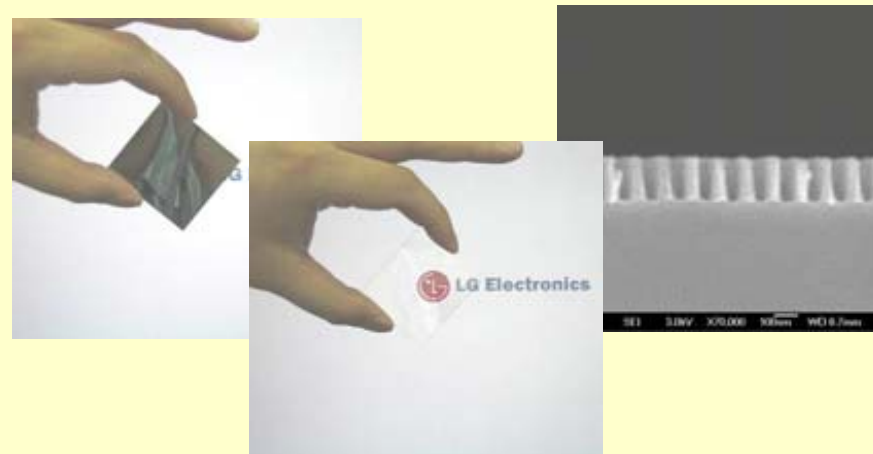
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Nanopatterning – Main NIL Applications

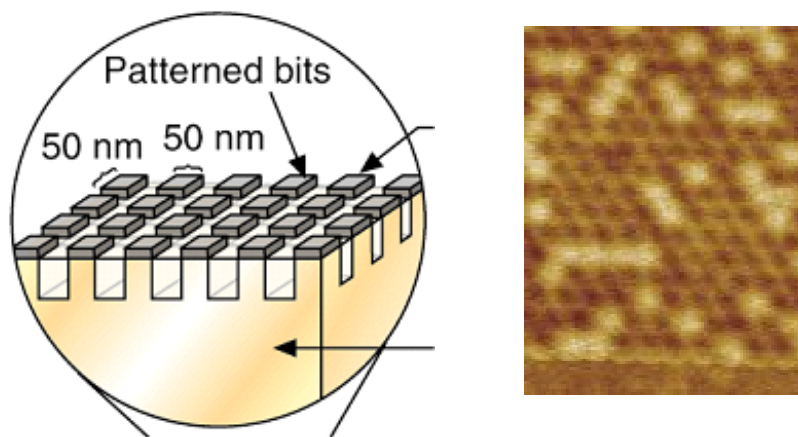
High End Microelectronic Chips



Wire Grid Polarizer



Patterned Magnetic Media



High Brightness LEDs

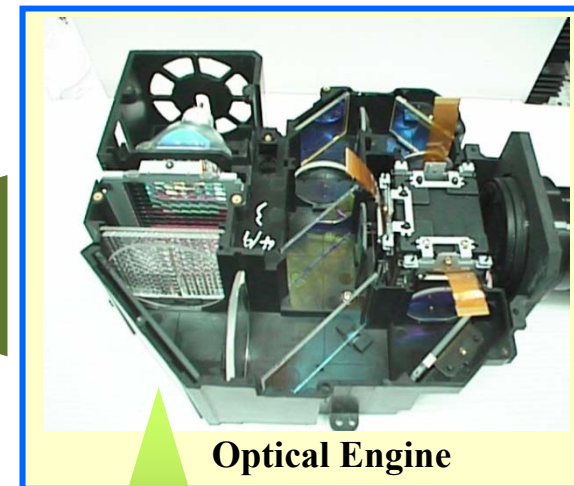


Wire Grid Polarizer in Projection Display

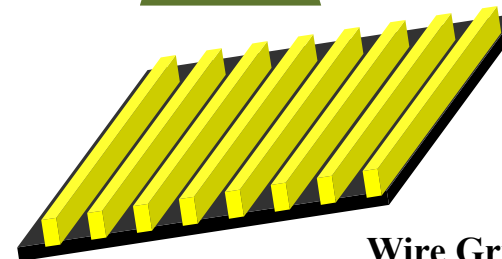
Wire grid polarizer is being increasingly adapted in micro-display projection TV as a core optical component.



LCD/LCoS Projection TV

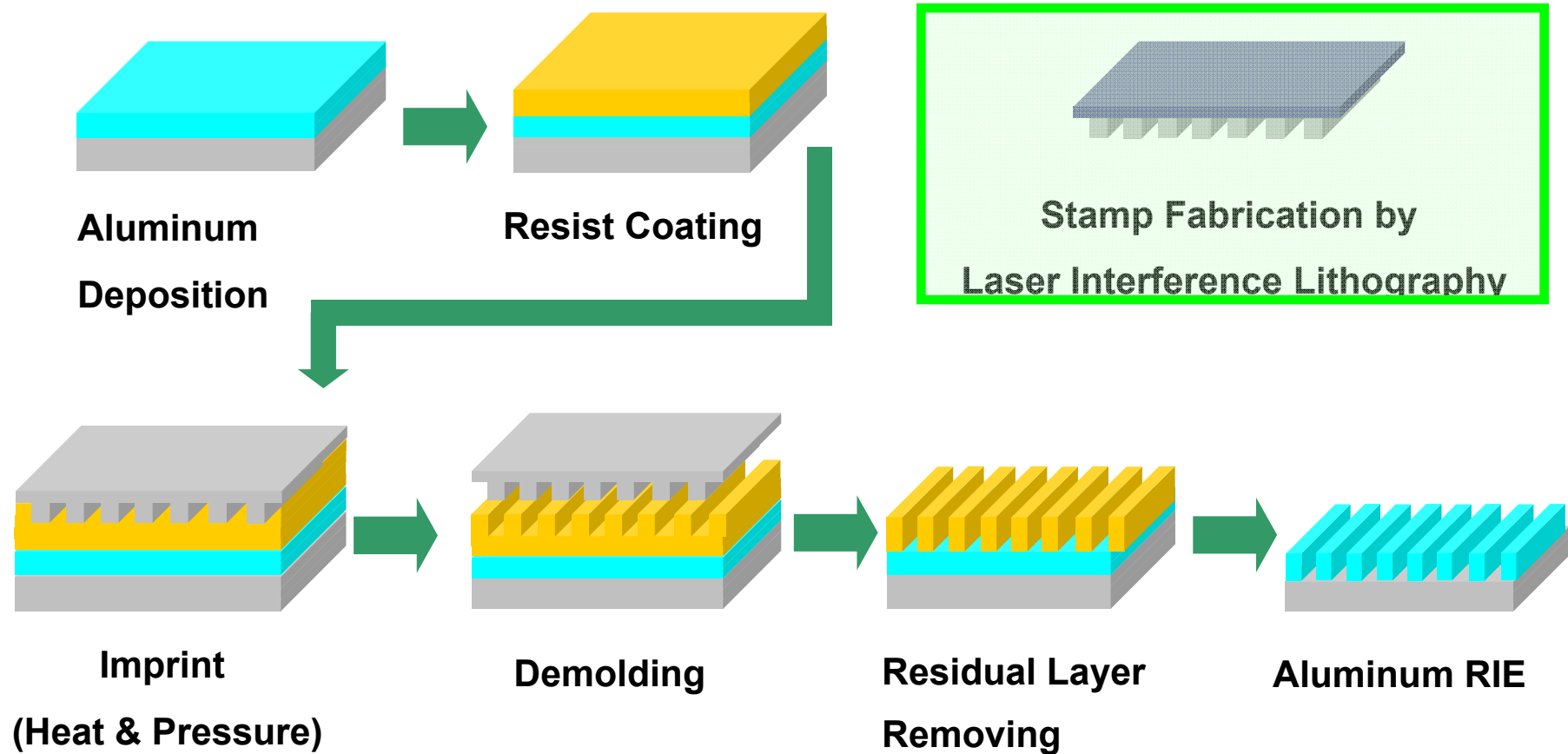


Optical Engine

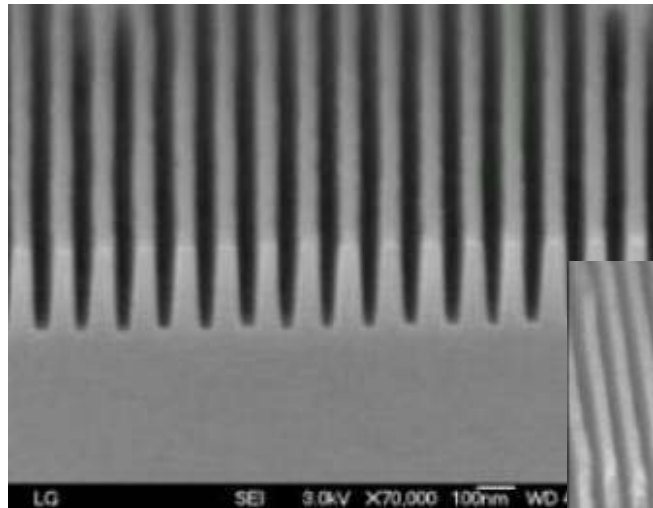


Wire Grid Polarizer

Fabrication Procedure

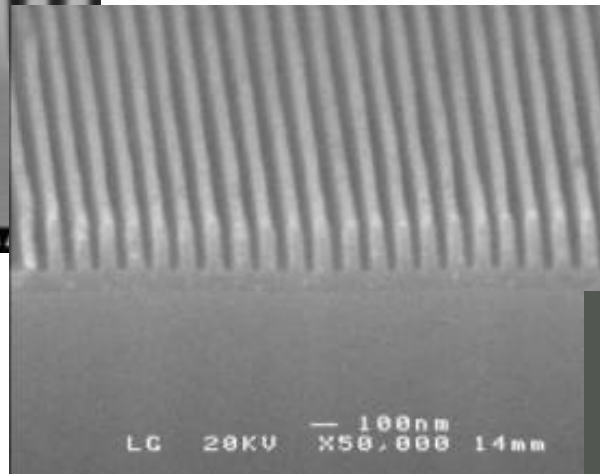


50 nm Half-pitch Gratings

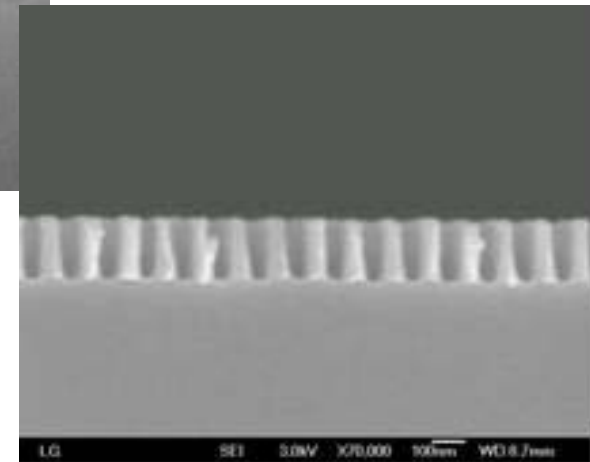


**Stamp with
50 nm half-pitch grating**

**Fabrication of 50 nm Half-pitch
Wire Grid Polarizer Using
Nanoimprint Lithography, NNT 2004**

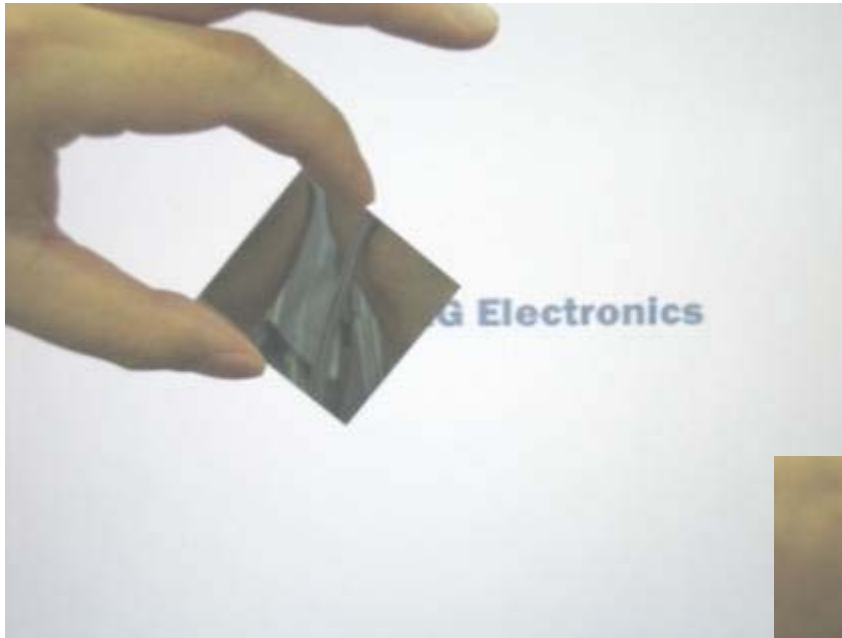


**Imprinted
polymer pattern**



50 nm half-pitch Al grating

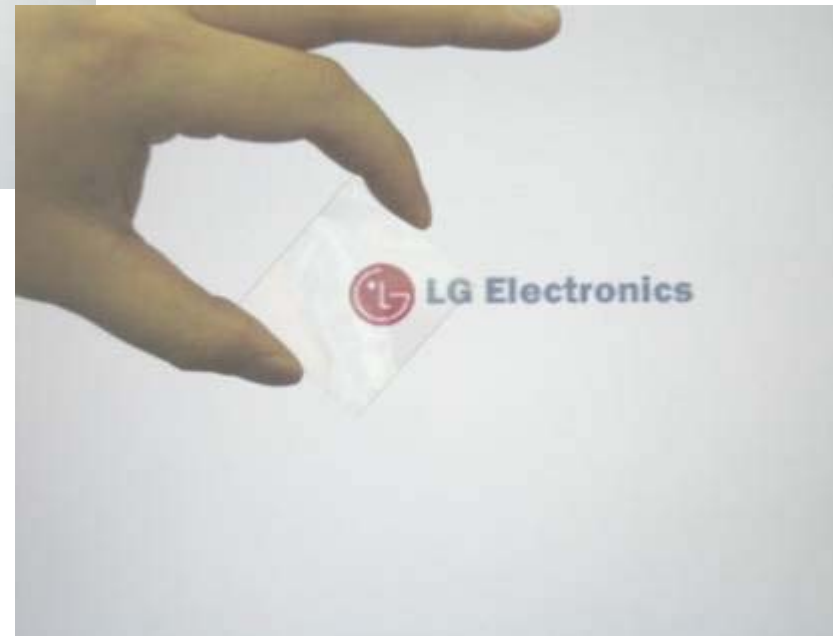
Performance of Fabricated Polarizer



Extinction Ratio > 2,000

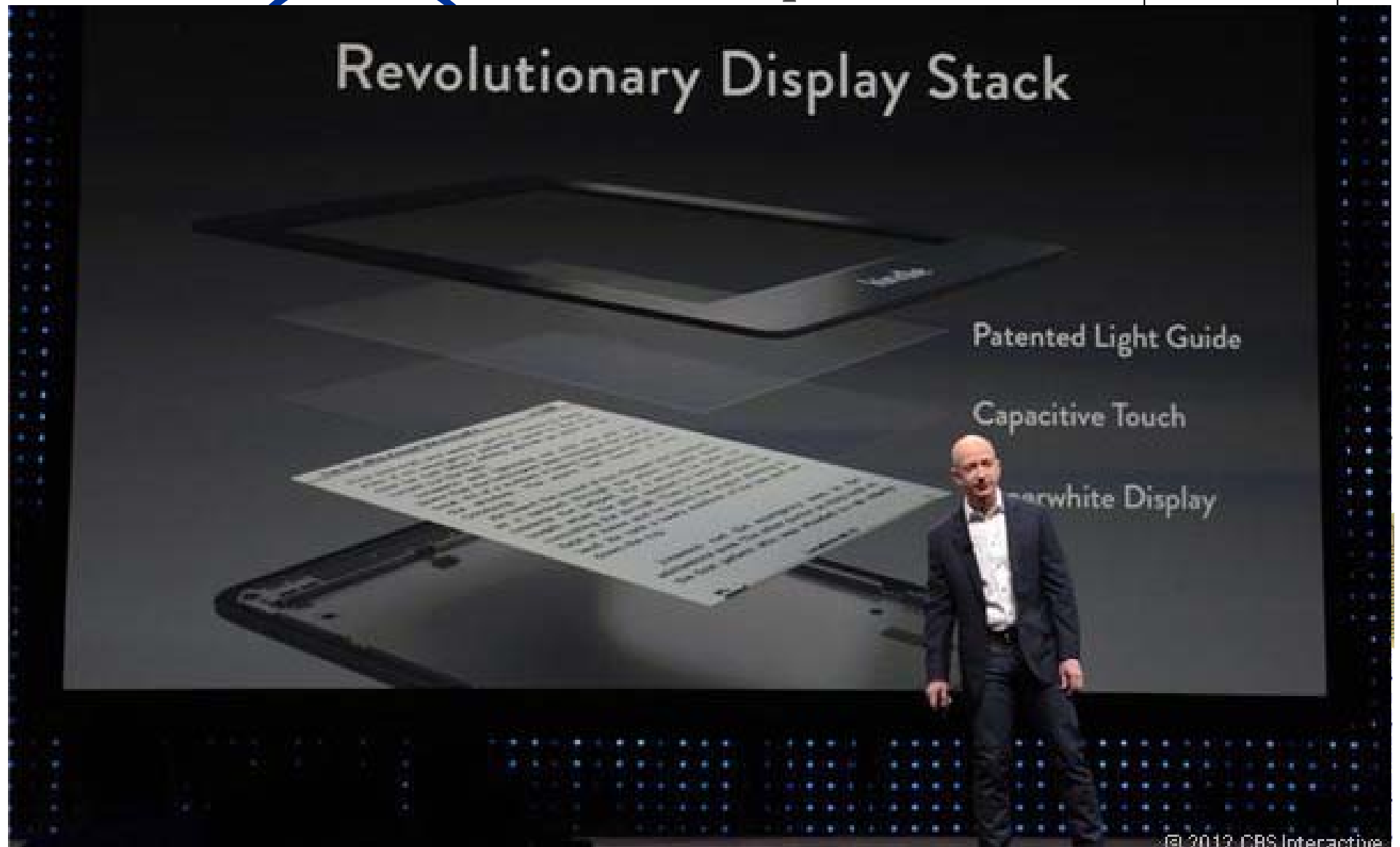
Transmission > 85 %

at $\lambda = 450 \text{ nm}$



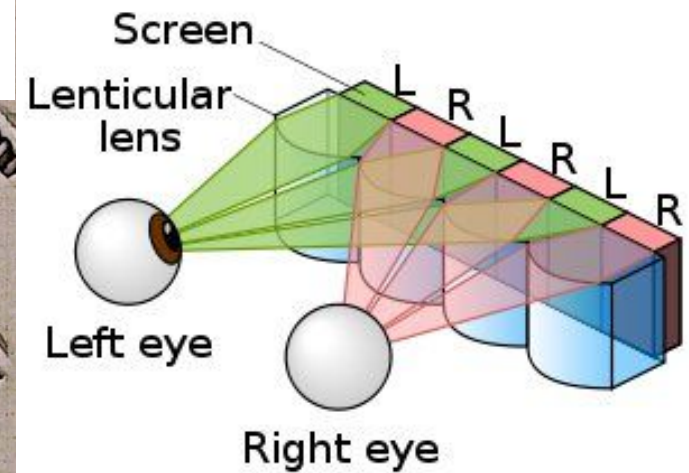
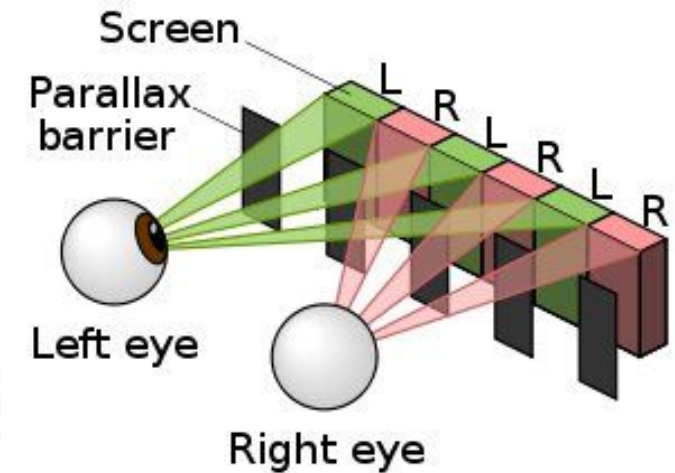
Industrial Demonstrators: Example 1 PDOE

Backlight



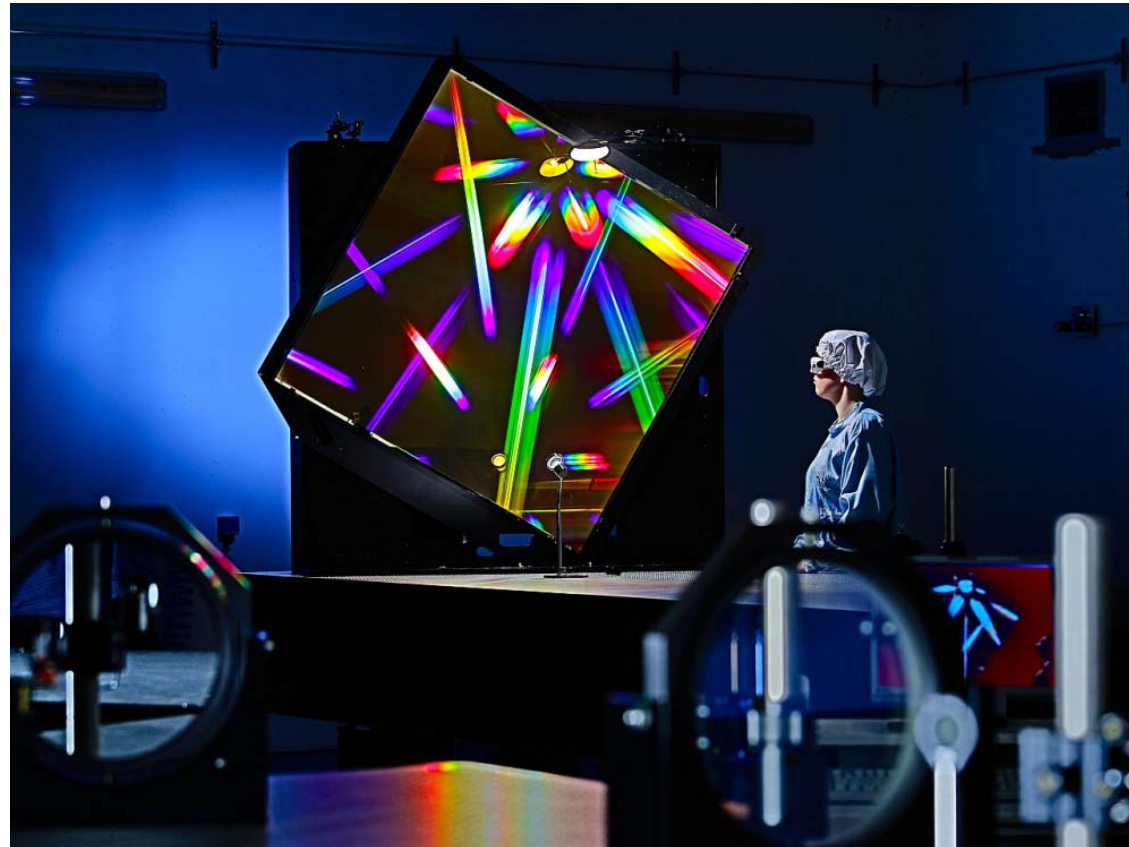
© 2012 CBS Interactive

EyeFly 3D Screen Protector from Nanoveu



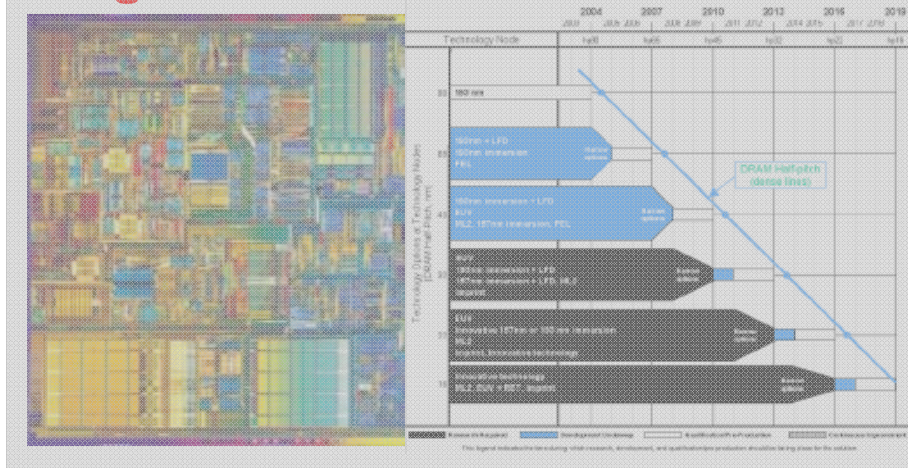
Structure Origination with Interference Lithography

- Maximum substrate size:
1.2 x 1.2 m²
- Exposure times:
up to 5 h
- Optical path lengths:
up to 20 m
- Acceptable instabilities: <
20 nm
- Extreme stability
requirements for building
and set-up

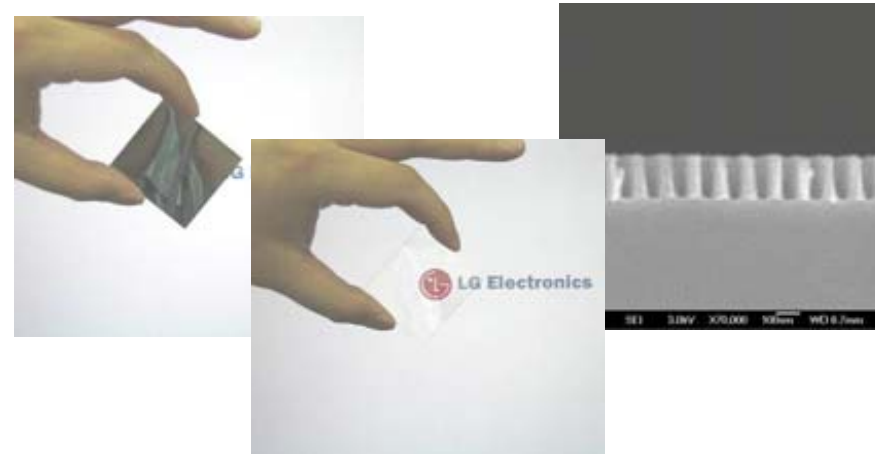


Nanopatterning – Main NIL Applications

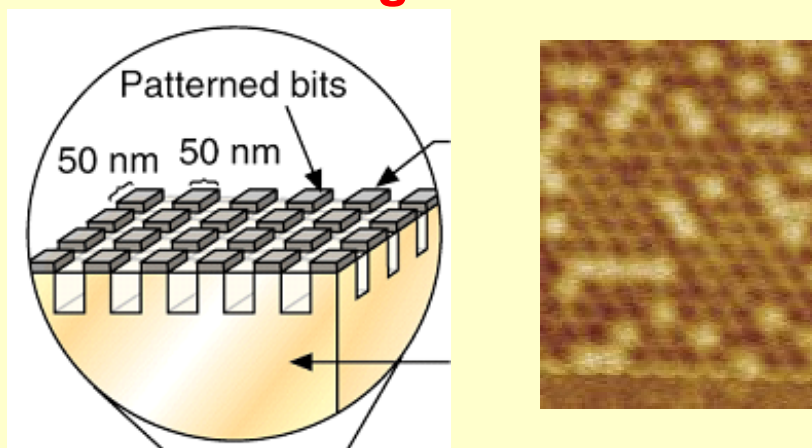
High End Microelectronic Chips



Wire Grid Polarizer



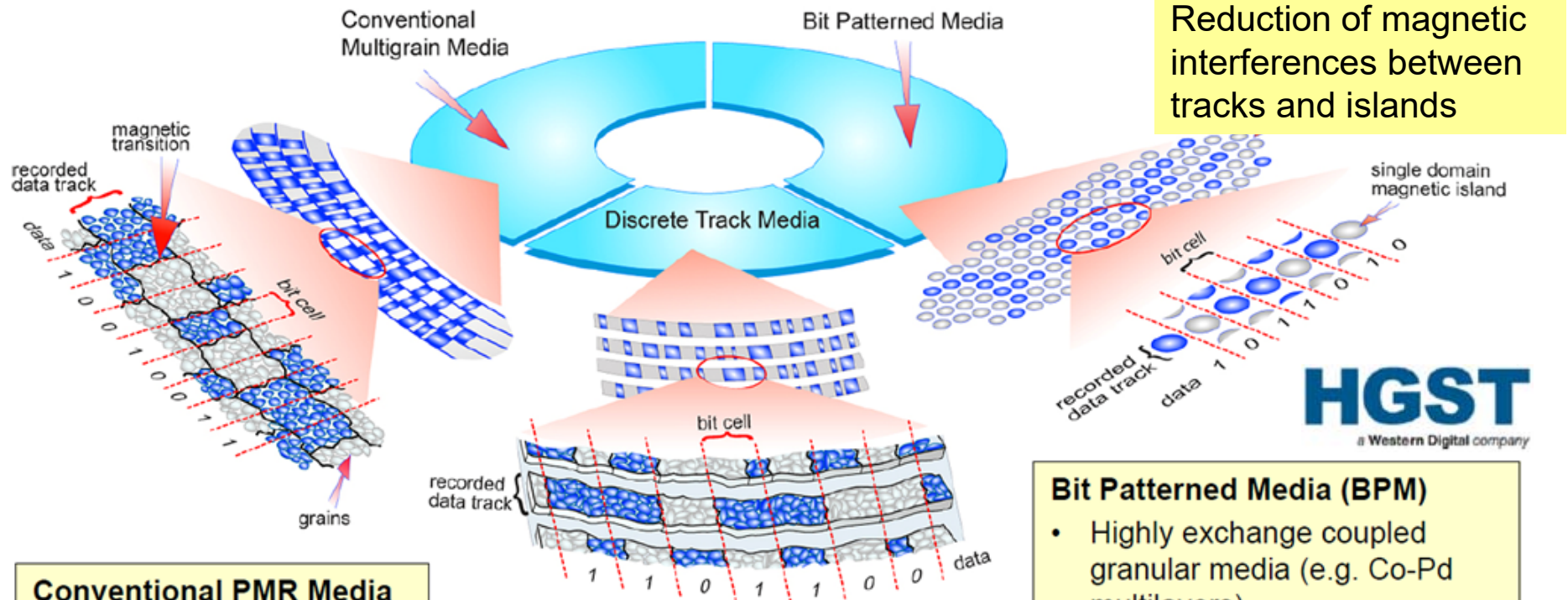
Patterned Magnetic Media



High Brightness LEDs



Conventional granular, discrete track, and bit patterned



Conventional PMR Media

- Continuous granular recording layer
- Multiple grains per bit
- Boundaries between bits determined by grains
- Thermal stability unit is 1 grain (~ 6 nm diam.)
- Reaching its limits

PMR = perpendicular magn. rec.

Discrete Track Media (DTM)

- Conventional PMR media, with patterned tracks
- Multiple grains per bit
- Eliminates track edge noise and reduces adjacent track interference
- Thermal stability unit is still 1 grain (~ 6 nm diam.)
- Modest areal density gain possible

Bit Patterned Media (BPM)

- Highly exchange coupled granular media (e.g. Co-Pd multilayers)
- Multiple grains per island, but each island is a single domain particle
- Bit locations determined by lithography
- Therm. stab. unit is 1 island (~15 nm diam.)
- Substantial areal density gain should be feasible

Magnetic Islands by Nanoimprinting

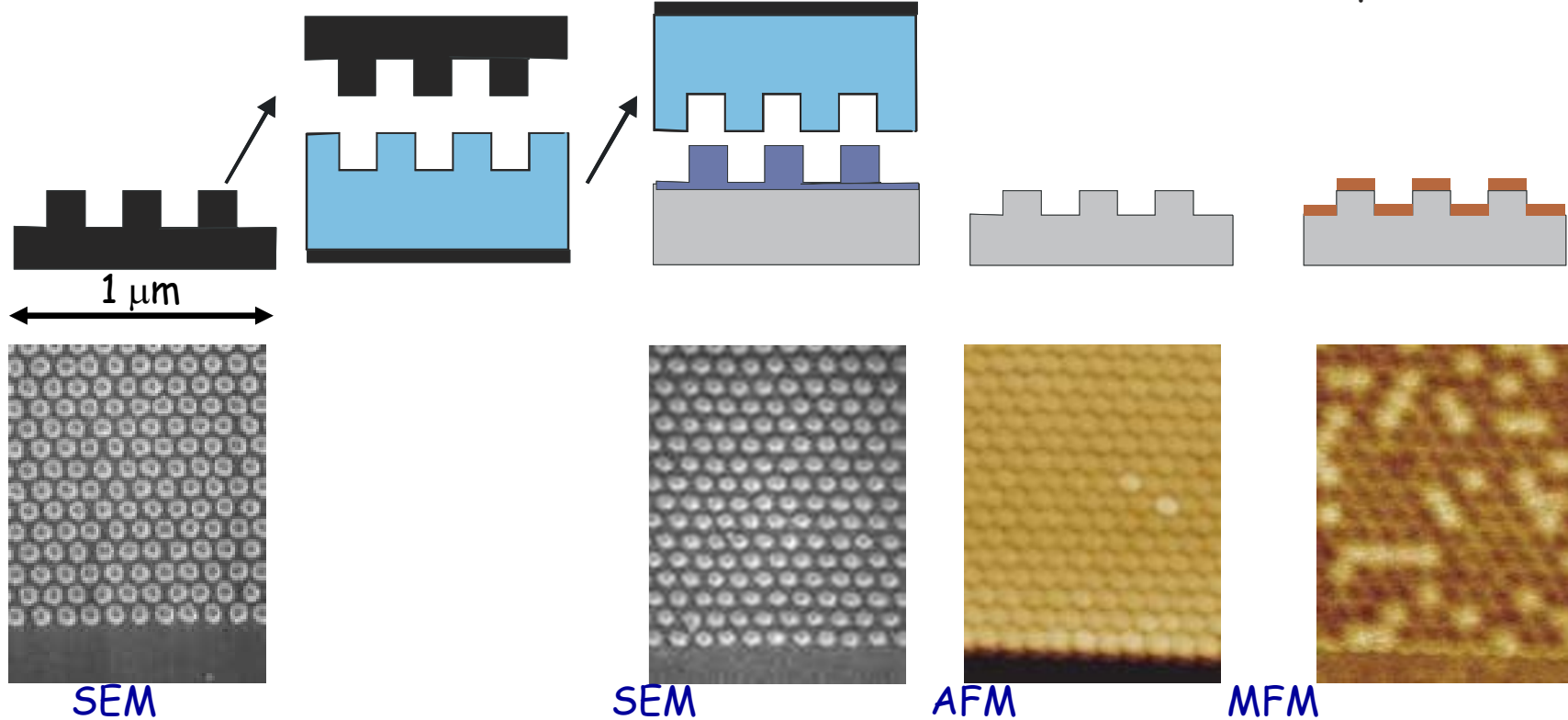
Make master
by e- beam
lithography

Form stamp
by photo-
polymerization

Form replica
by photo-
polymerization

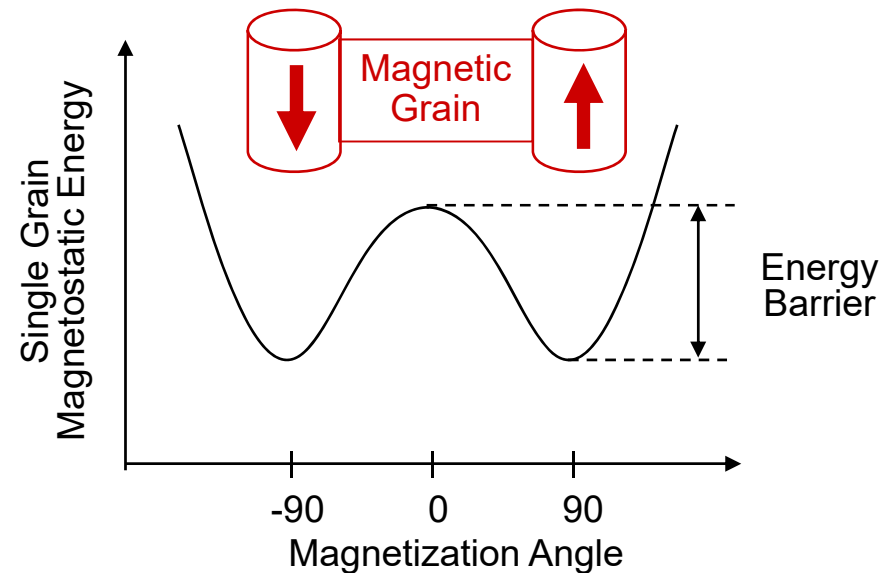
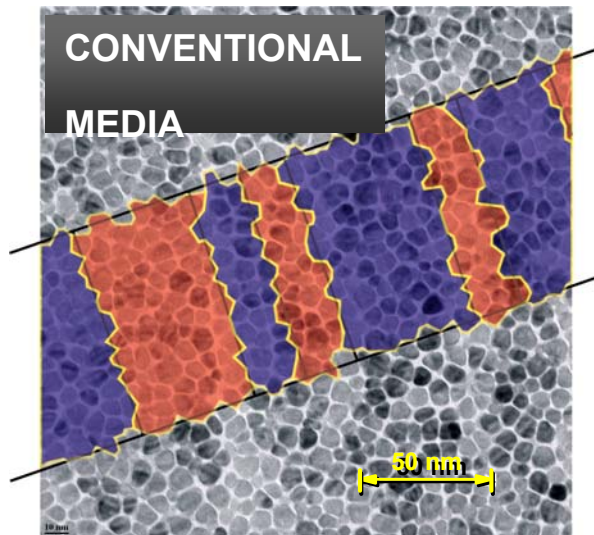
Transfer
Pattern by
RIE

Deposit CoPt
Multilayer by
Evaporation



Source: Hewlett Packard, NNT2004

The problem: thermal stability, write-ability, and density



Magnetic Stability: $\frac{\text{energy barrier}}{\text{thermal energy}} \propto \frac{\text{anisotropy} \times \text{volume}}{k_B \times \text{temperature}} = \frac{K_u V}{k_B T} > 70$

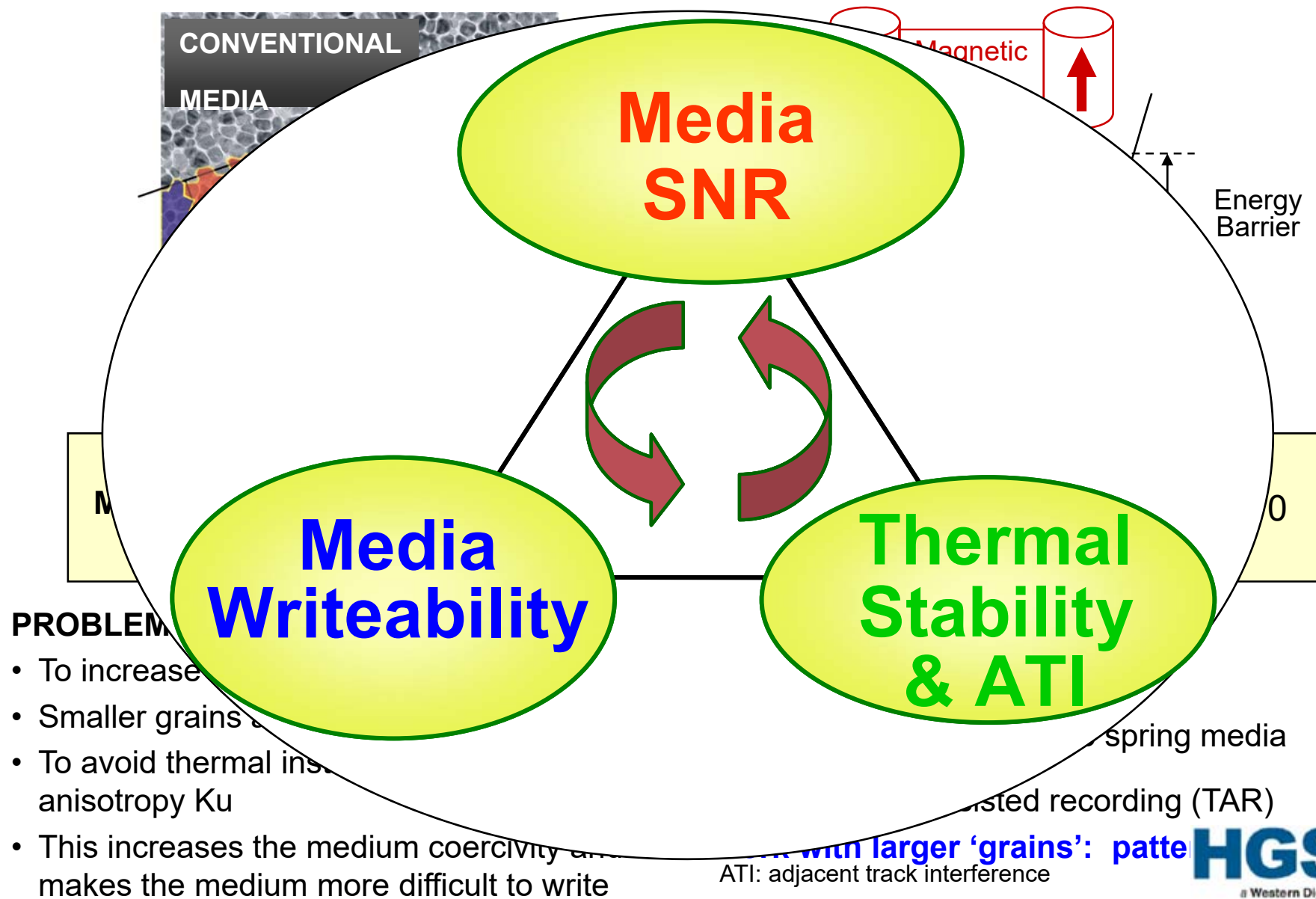
PROBLEM:

- To increase density, need smaller grains
- Smaller grains are thermally unstable
- To avoid thermal instability, increase grain anisotropy K_u
- This increases the medium coercivity and makes the medium more difficult to write

SOLUTIONS:

- Work with higher anisotropy:
 - Capped and exchange spring media
 - Thermally assisted recording (TAR)
- **Work with larger 'grains': patterned media**

The "Trilemma"

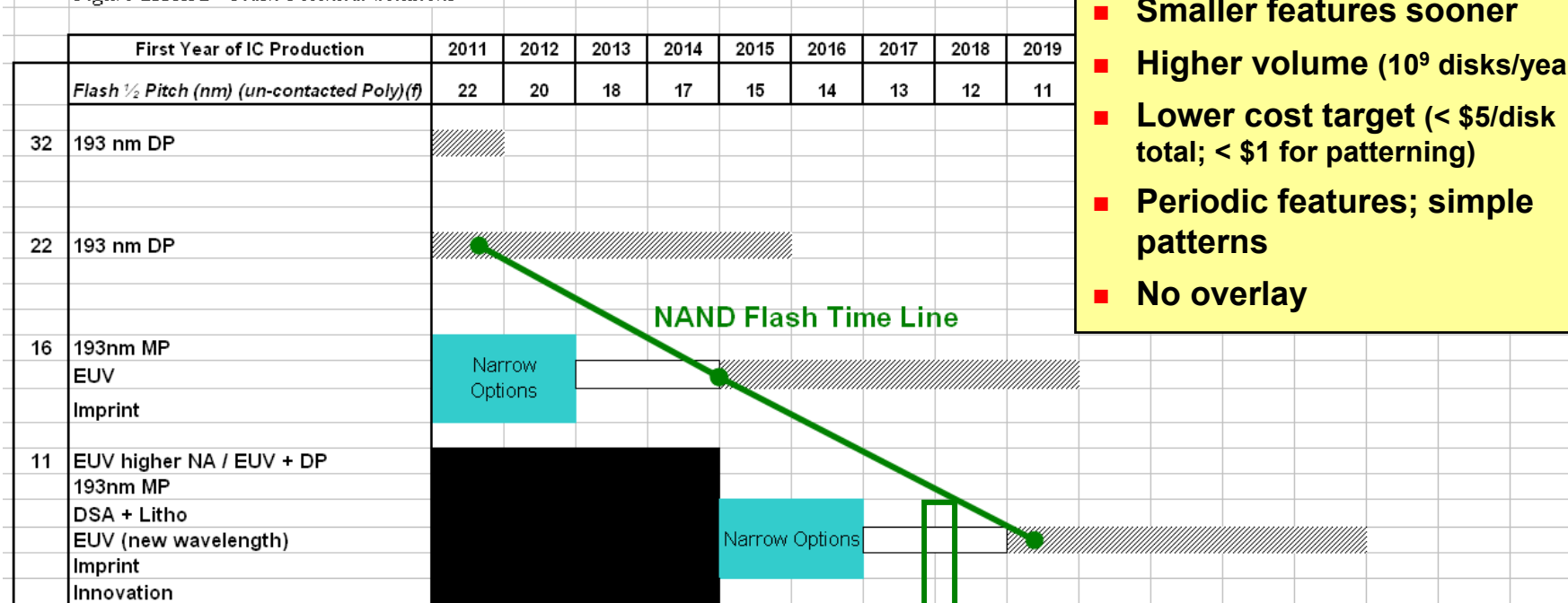


BPM Requires Features Smaller Than Semiconductors



International Technology Roadmap

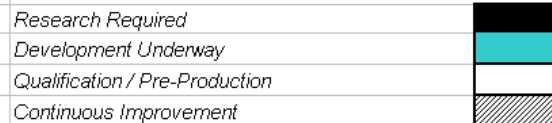
Figure LITH3B Flash Potential Solutions



Compared to semiconductor manufacturing, we need:

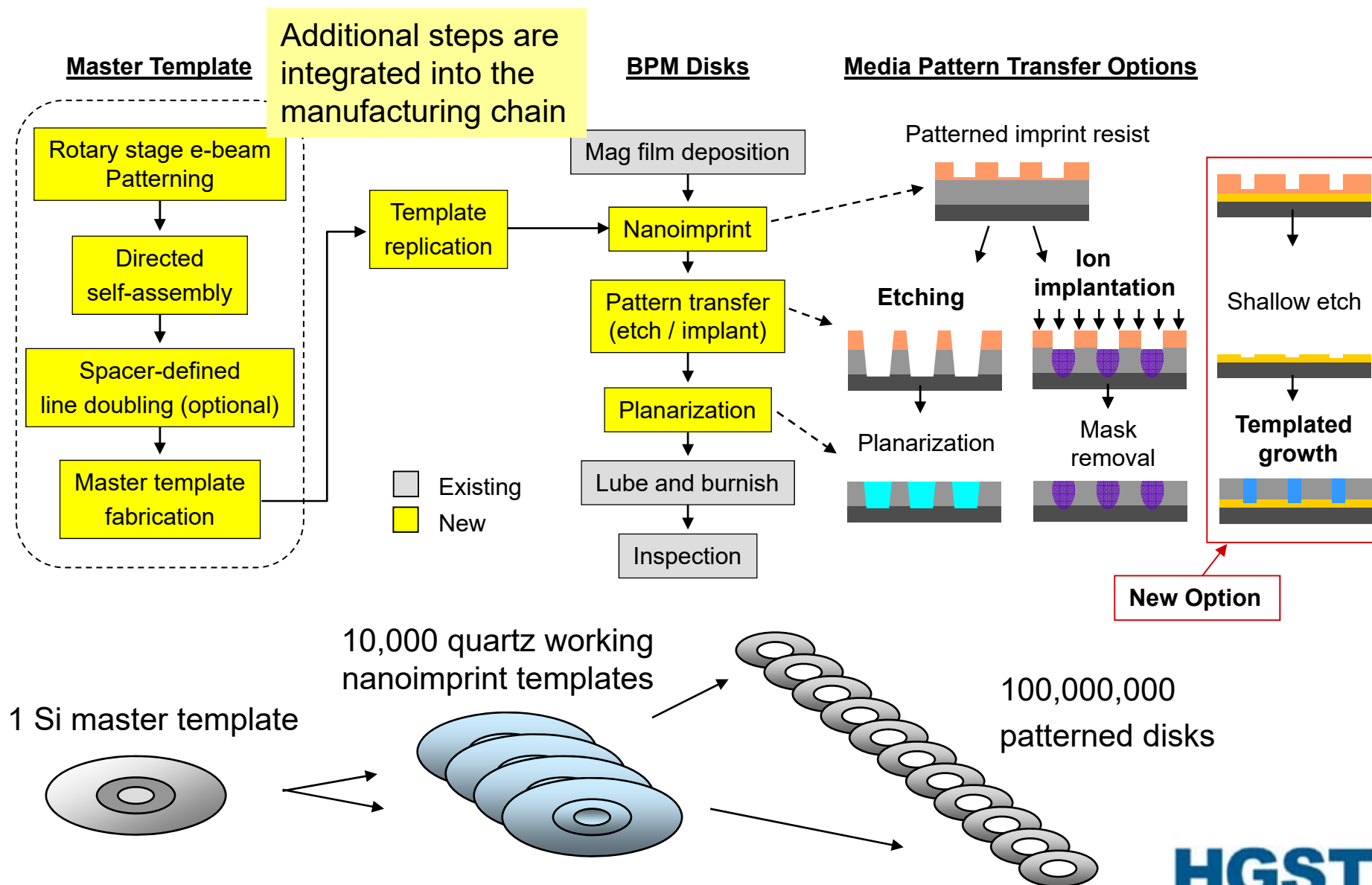
- Smaller features sooner
- Higher volume (10^9 disks/year)
- Lower cost target (< \$5/disk total; < \$1 for patterning)
- Periodic features; simple patterns
- No overlay

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.



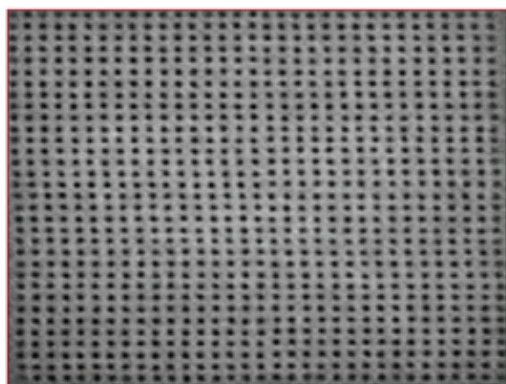
6-9 nm needed

BPM High Volume / Low Cost Fabrication Strategy



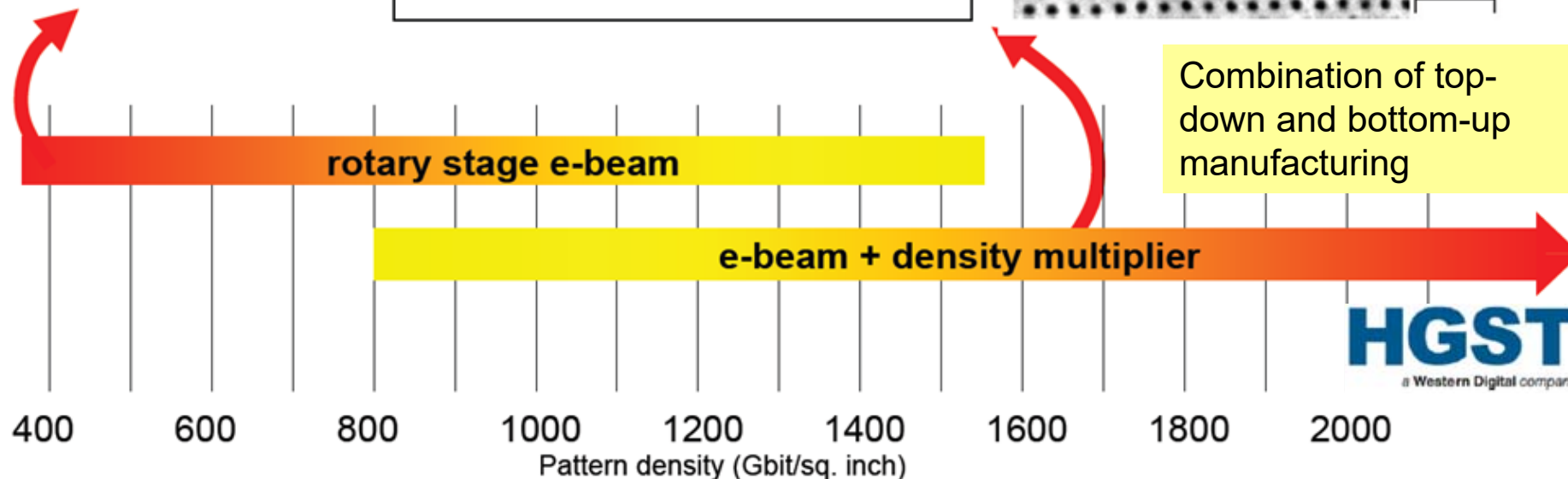
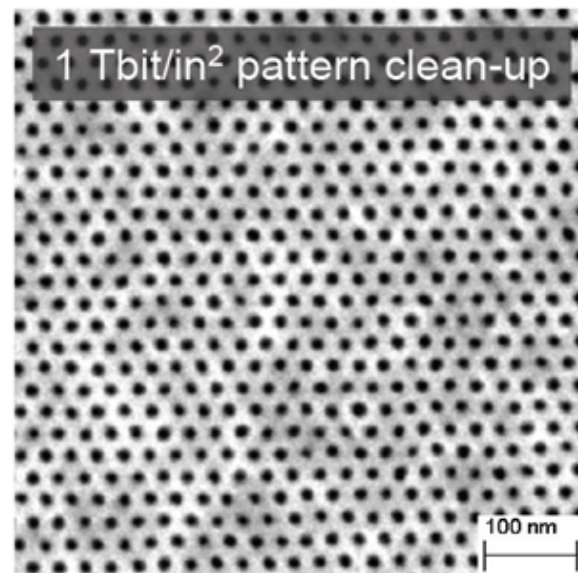
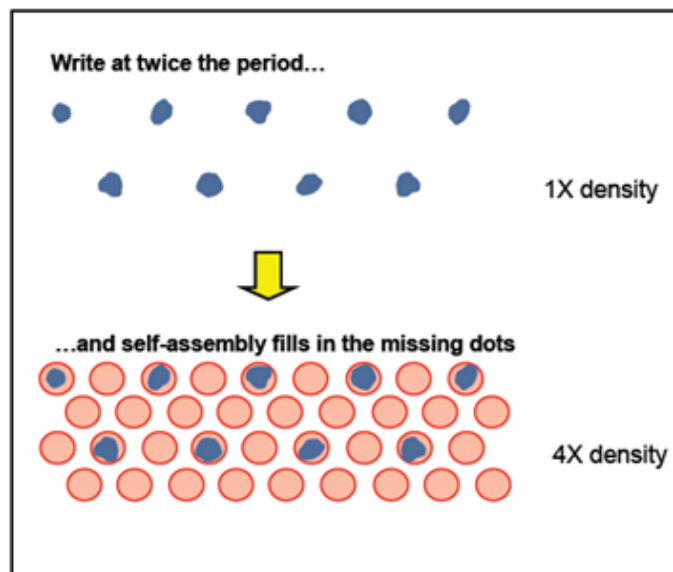
Master pattern lithography roadmap

E-beam lithography



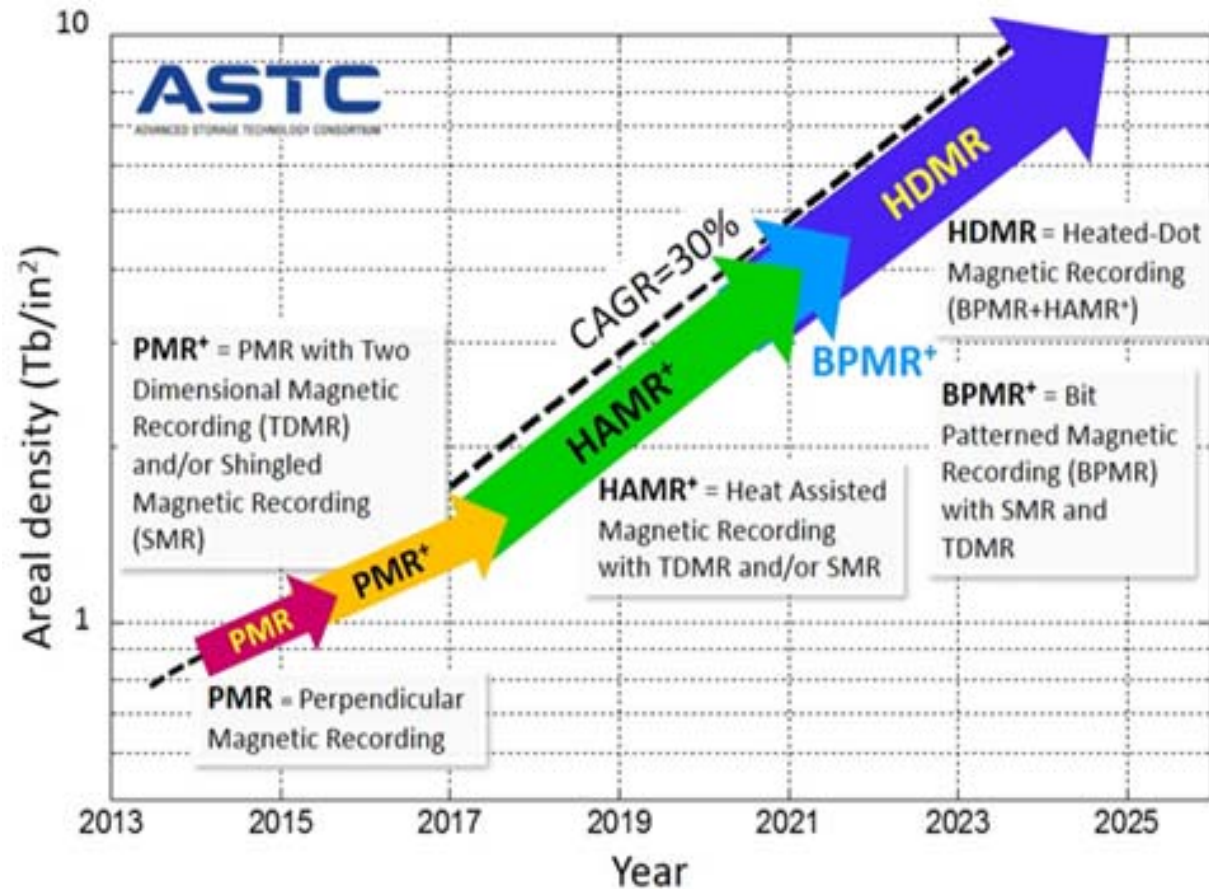
720 Gbit/in² (30 nm period):
Holes etched in Si master mold
(Leica VB-6 100 kV w/ PMMA, cold
ultrasonic develop; RIE pattern transfer)

e-beam prepattern + block copolymer self-assembly



HGST
a Western Digital company

BPM-Status: it is on in the industry roadmap



Bit-patterned media is on the ASTC industry roadmap for post-2020

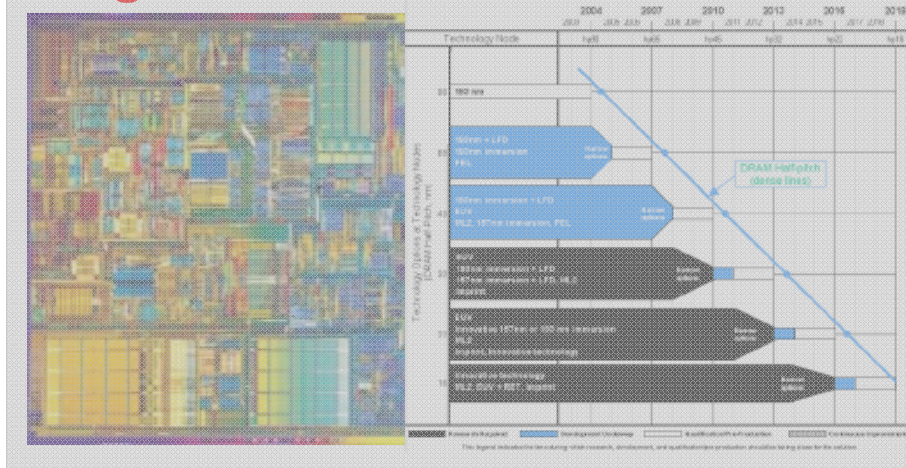
WesternDigital (HGST): BPM «on hold» (last publication 2015)

Seagate: still active in BPM (last publication 2015)

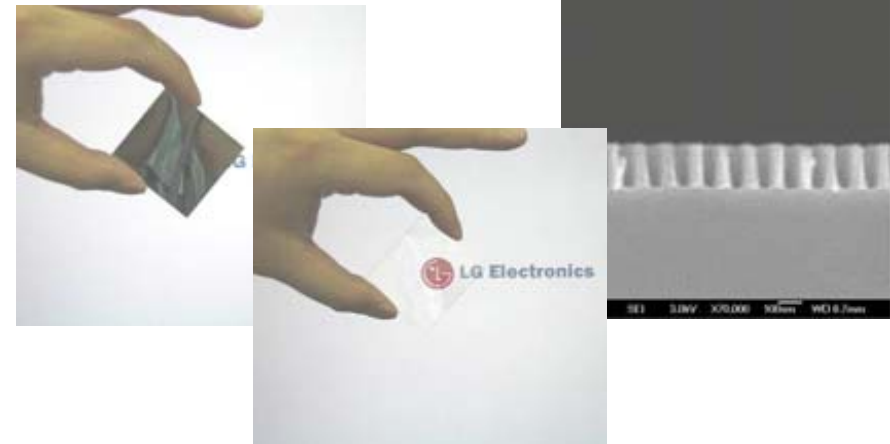
Toshiba: ? (last publication 2010)

Nanopatterning – Main NIL Applications

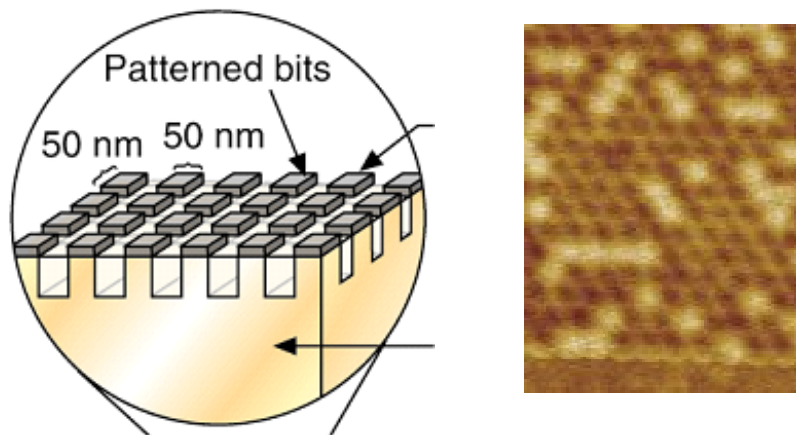
High End Microelectronic Chips



Wire Grid Polarizer



Patterned Magnetic Media



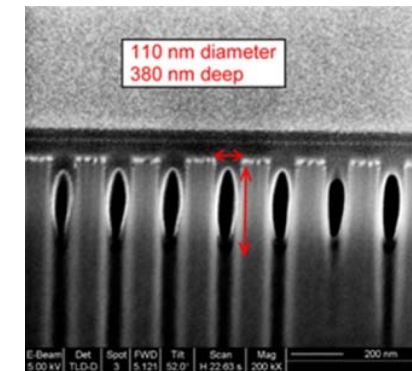
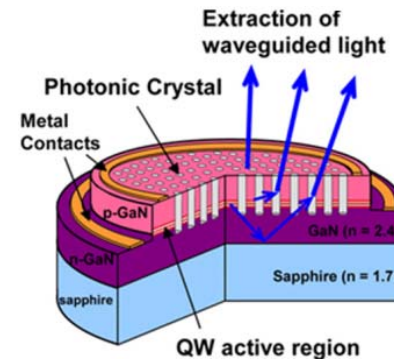
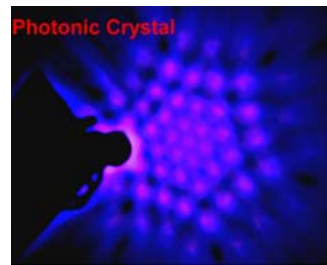
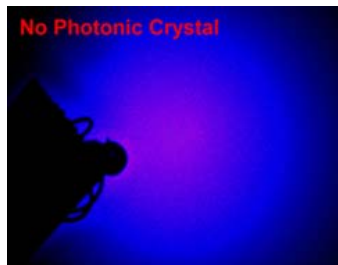
High Brightness LEDs



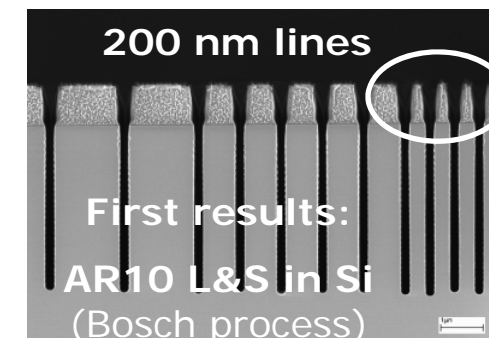
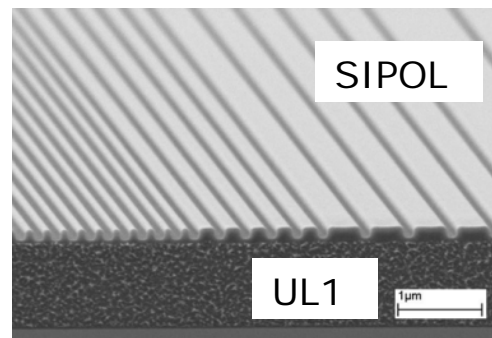
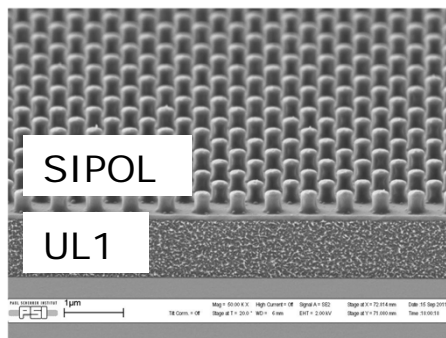
Different concepts for the realization of high-brightness LEDs

1. Photonic crystals

High aspect ratios in GaN necessary ($>3:1$)

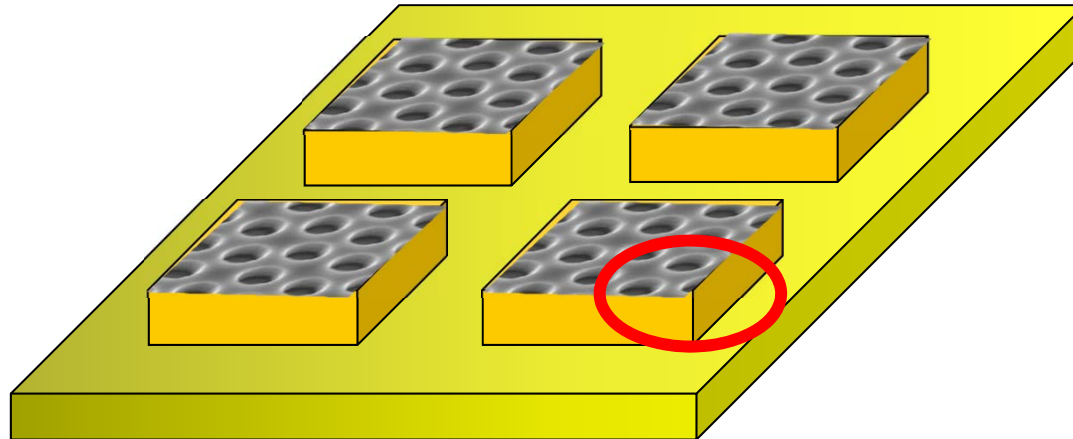


e.g. SIPOL in a bilayer approach



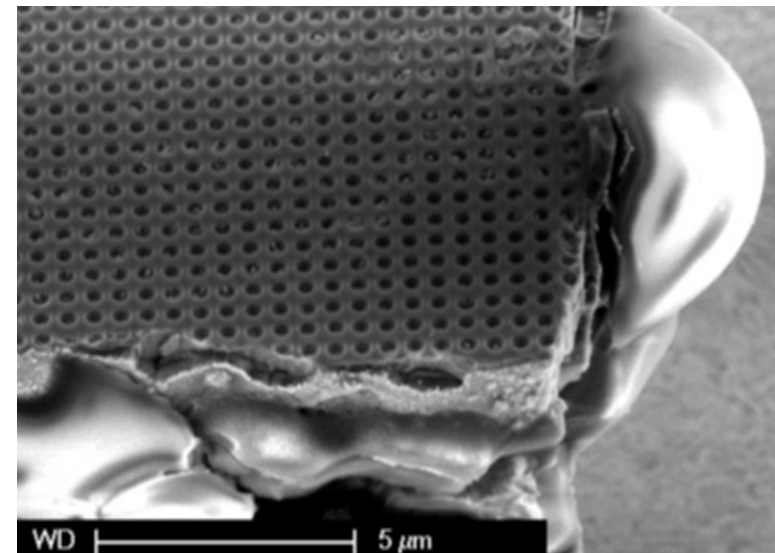
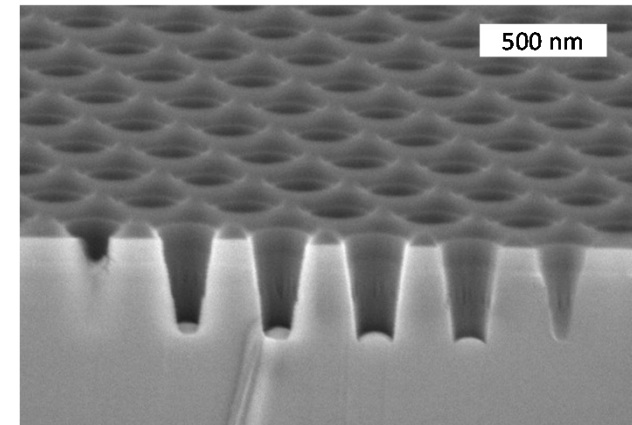
DL Barton and AJ Fischer SPIE
Newsroom **2006**
doi: 10.1117/2.1200603.0160

Patterning LEDs on sub-mount



Separated LED chips

- Test LEDs
- Place individual LEDs
- Spray coat sol-gel resist
- Flexible stamp
→ Imprint on top of LEDs
- Etch GaN



Courtesy of: M. Verschuuren, Philips Research, Eindhoven

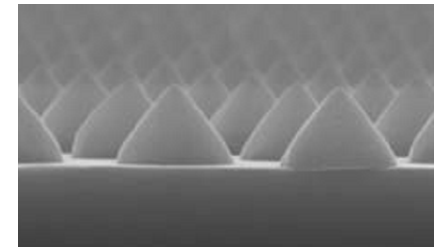
Different concepts for the realization of high-brightness LEDs

2. Nano-Patterned Sapphire Substrates (NanoPSS)

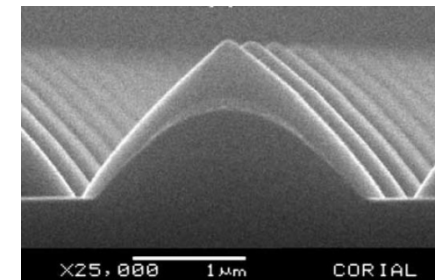
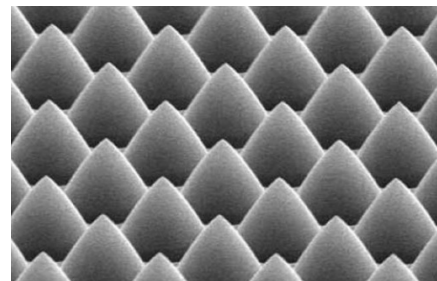
Concept with the widest use in industry

Hemispheres, cones, triangles, hexagons, etc...

- mr-NIL 6000E, mr-I 9000M
- **PSS-specific Photo-NIL resist prototypes** (PDMS compatibility)



Y-C Lee and S-H Tu *Rec Adv in Nanofabrication Techn and Appl* 173
2011 196

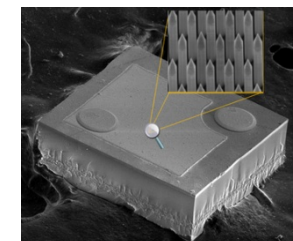


www.corial.net

3. Nano-wire approach

True white light LED chip possible without the need of an additional phosphor

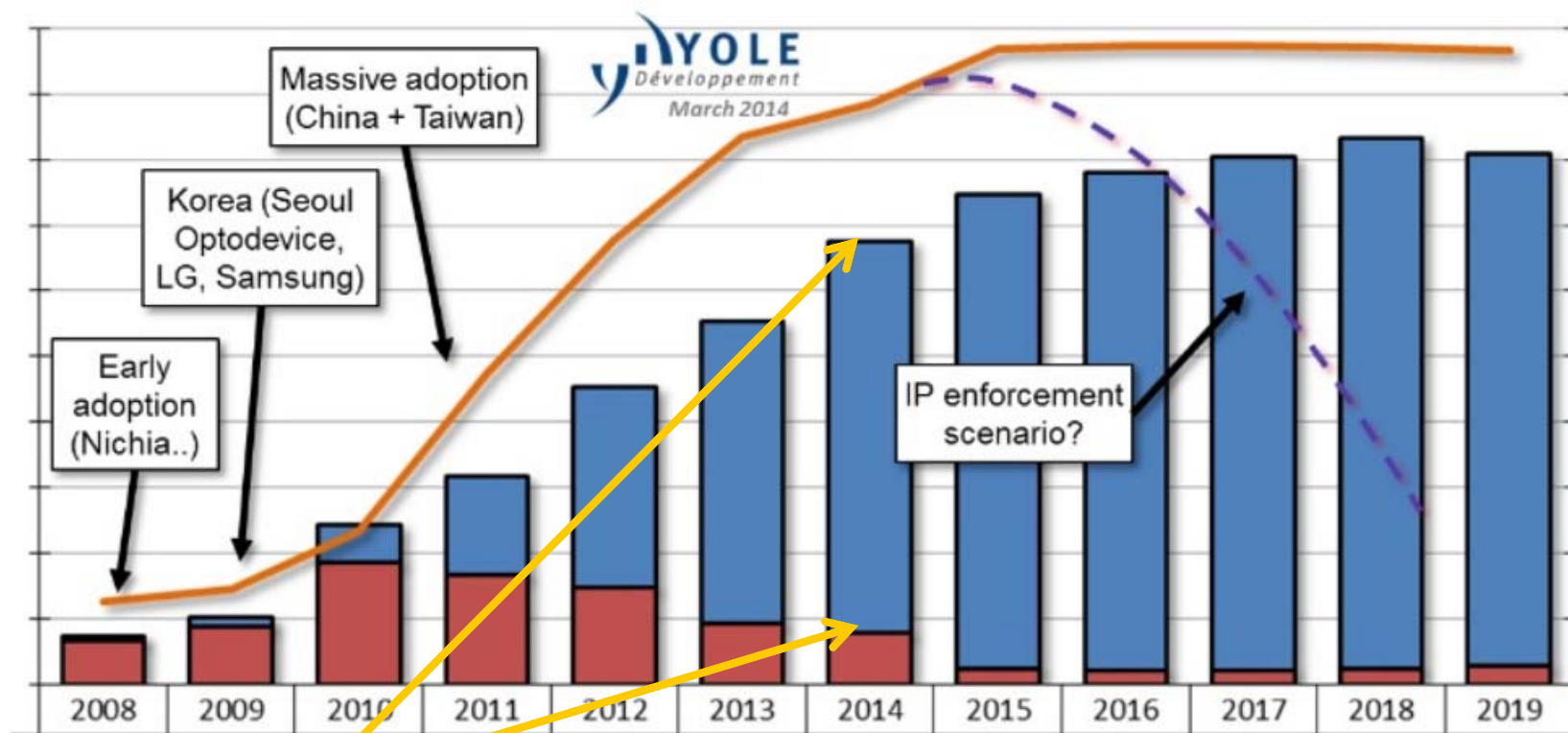
mr-NIL 6000E, mr-I 9000M



www.glo.se

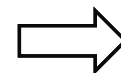
Nano-Patterned Sapphire Substrates (NanoPSS)

PSS and Standard Substrate Volume (2008 - 2018)



87% of fabricated LEDs in 2014 are processed on PSS

PSS: optical Lithography



Nano-PSS requires NIL

Nanoimprint Machines from SÜSS : MA8-SCIL



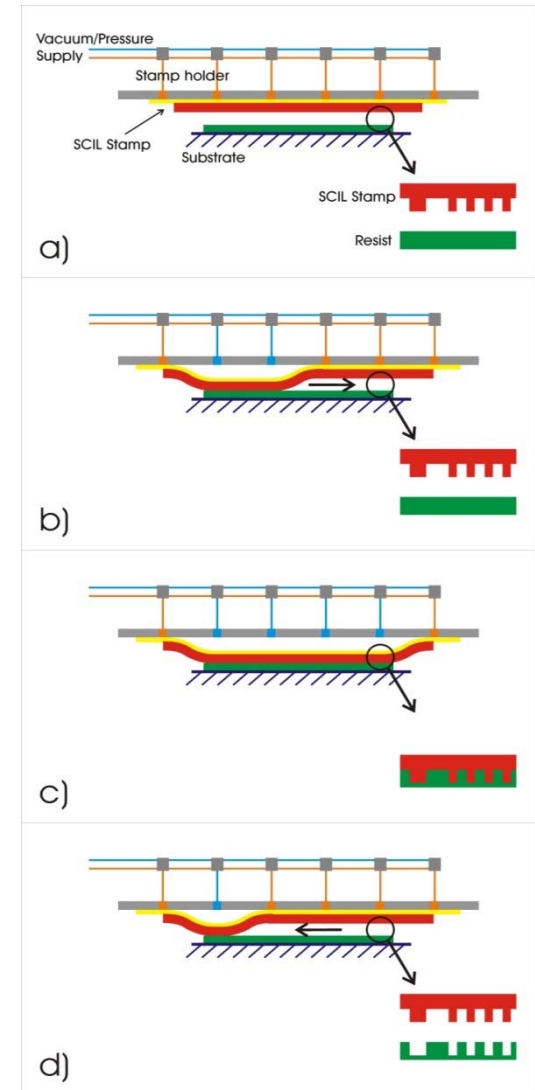
6"-8" imprint tool at AMO / Aachen

- UV imprint of large areas
- alignment

MA8-SCIL tool:

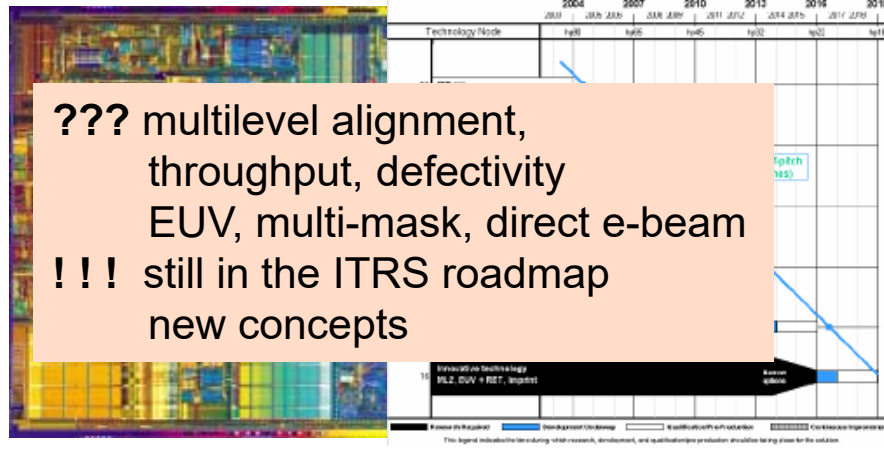
- Substrate Conformal Imprint Lithography (SCIL)
- Composite soft stamps
- Demonstrated with UV-curable resists and Sol-gel materials
- Semiautomatic tool
- 1000 W lamp
- 6 & 8 inch system
- Alignment system

(+) molding and demolding
(-) layered stamp needed

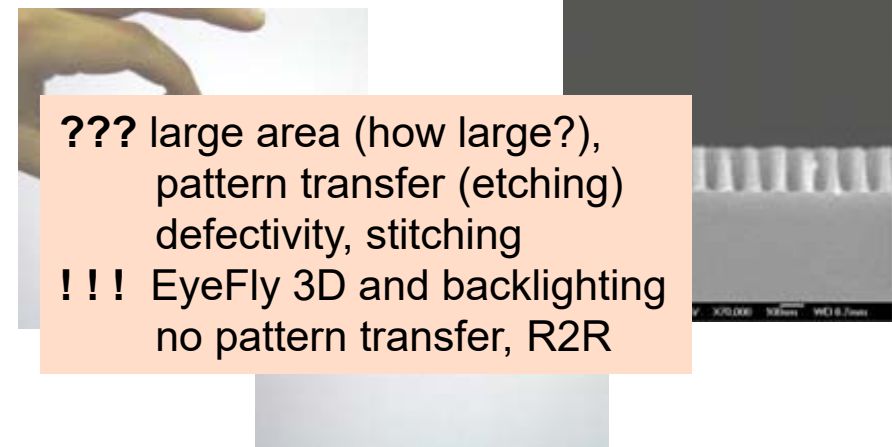


Nanopatterning – Main NIL Applications

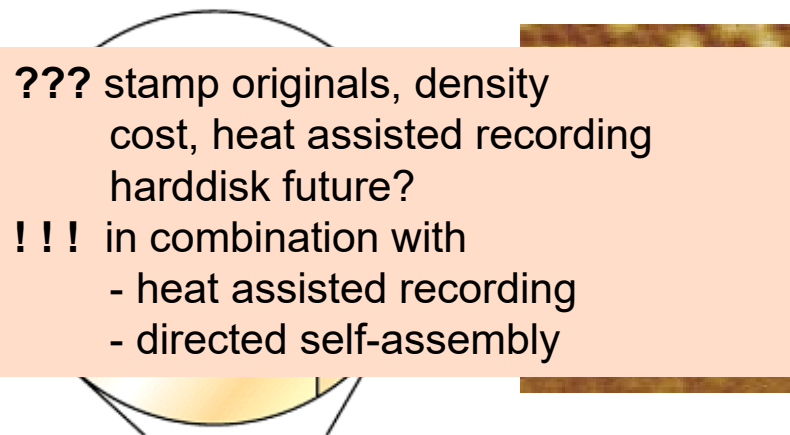
High End Microelectronic Chips



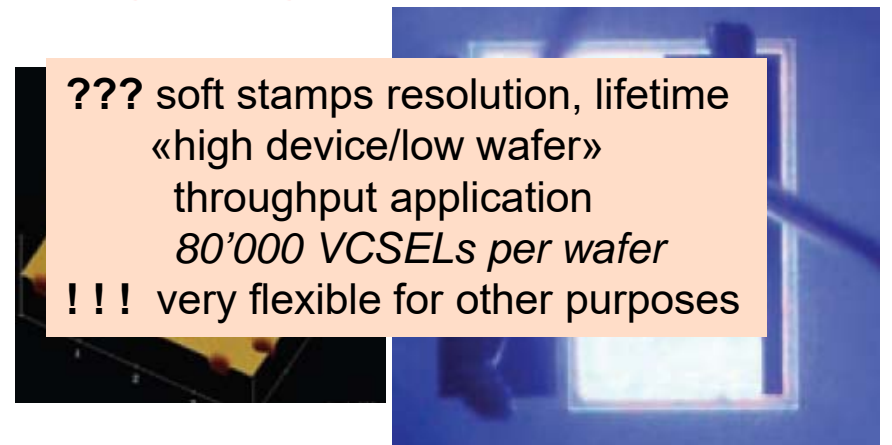
Wire Grid Polarizer



Patterned Magnetic Media



High Brightness LEDs



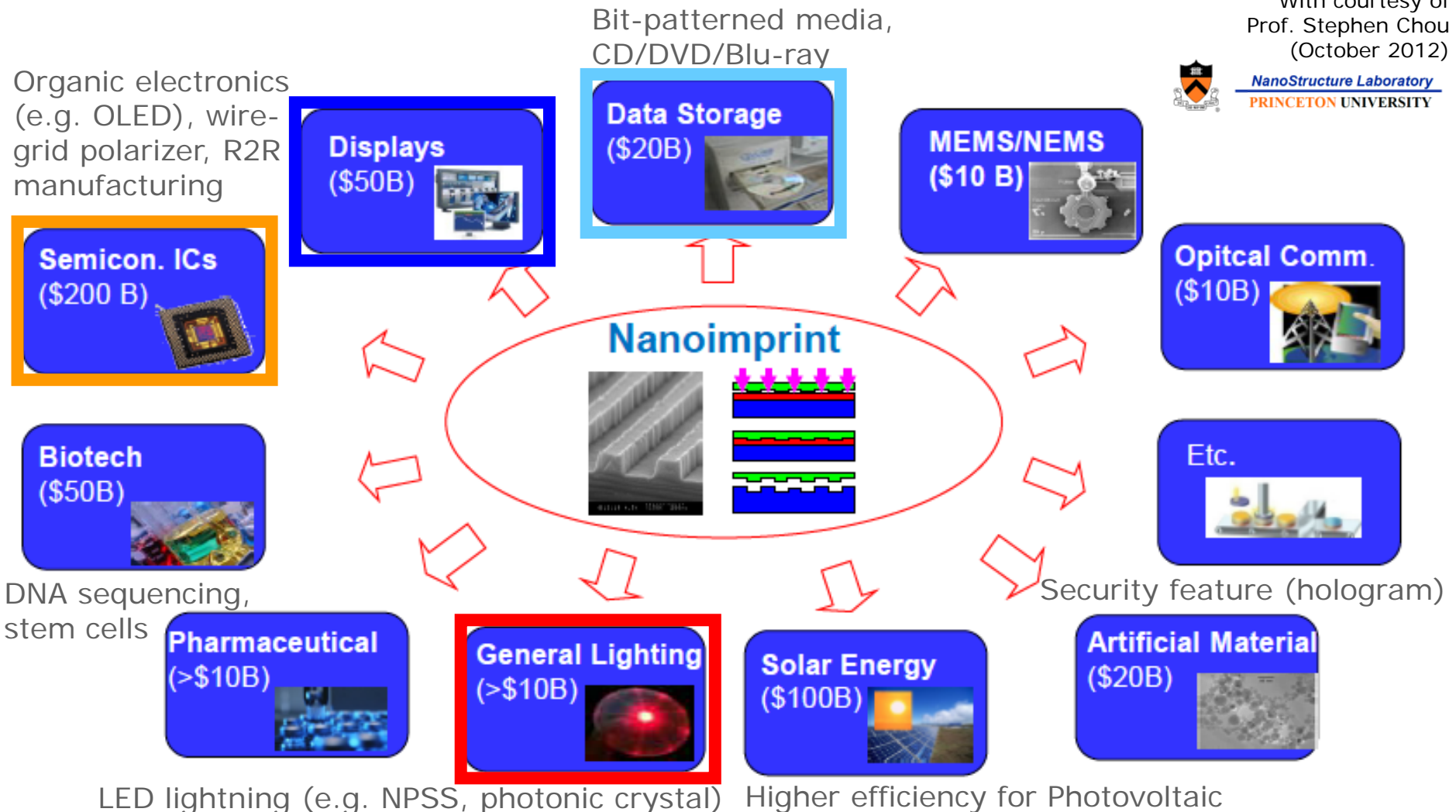
Nanoimprint enables Multi-billion Dollar Industries

Easy 3D patterning of functional materials using NIL technology

With courtesy of
Prof. Stephen Chou
(October 2012)



NanoStructure Laboratory
PRINCETON UNIVERSITY



Outline

- Nanoimprint in the context of advances in mechanical engineering
- NIL is a **N**ext **G**eneration **L**ithography – true, but not only!
- Is NIL More Moore or More than Moore?
- Non-IC applications, more than Moore – front runners
- What a researcher can contribute
- ... and **More NIL** to come

Application Examples (non-IC)

Electronics

- High brightness LEDs
- Photovoltaics
- Energy Storage (Li-Ion Batteries)
- Thin Film Transistors (TFTs)
- Lasers
- Structuring of Graphene
- Nanostructured Photoelectrodes

Pharmaceutics/Bioapplications

- Plasmonic Biosensors
- Titanium Implants

Optics

- Wire Grid Polarizers (WGPs)
- Metamaterials
- Sub-15 nm metal gratings
- Microlenses with nanostructures

Data storage

- Bit patterned (magnetic) media
- Crossbar storage

MEMS/NEMS

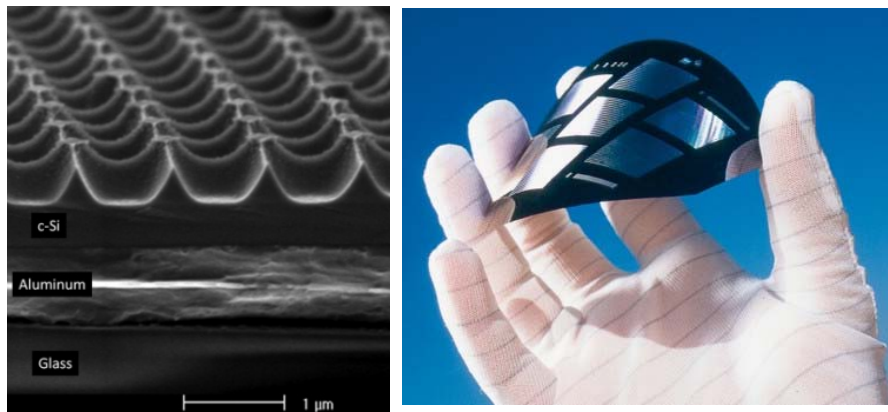
- Write/read heads
- Microcantilevers / -membranes

- Micro- and nanofluidics
(μ TAS, DNA sequencing, ...)
- Biomimetic structures

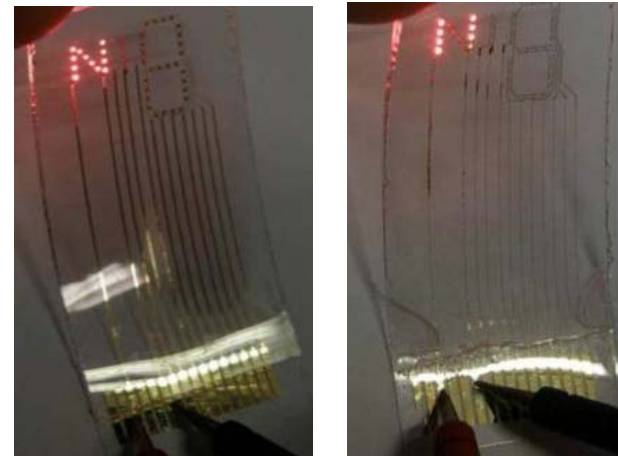
- Fishnet transparent electrodes
- Structural colors
- Backlight display waveguides
- Light redirection for lighting
- Liquid crystal cells for displays

Nanopatterning – Main NIL Applications

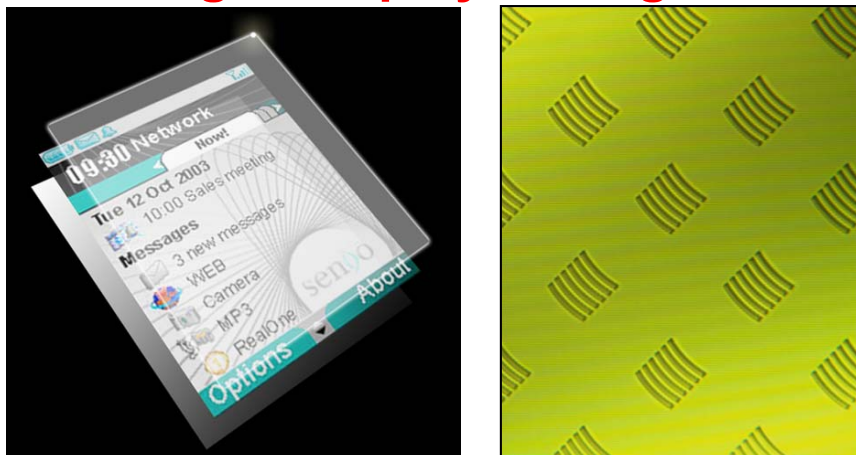
Photovoltaics



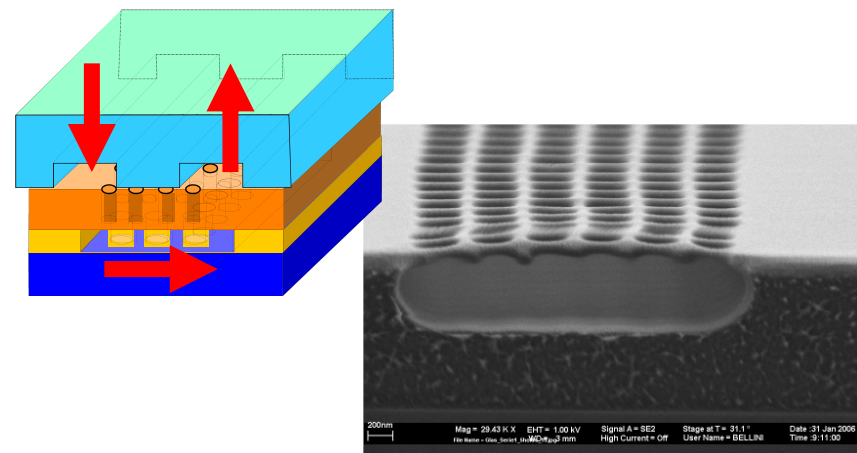
Transparent electrodes



Backlight Display Waveguides

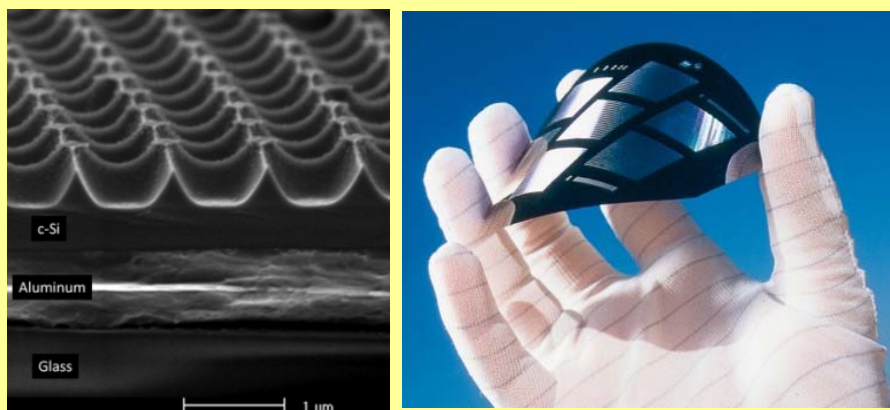


Nano-Fluidic Devices

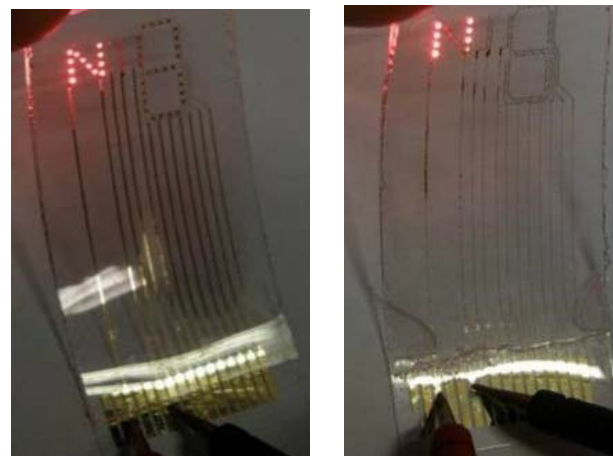


Nanopatterning – Main NIL Applications

Photovoltaics



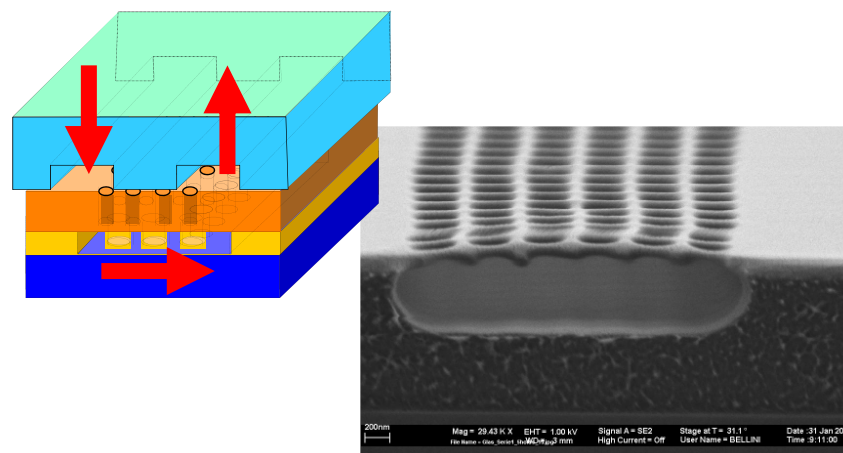
Transparent electrodes



Backlight Display Waveguide

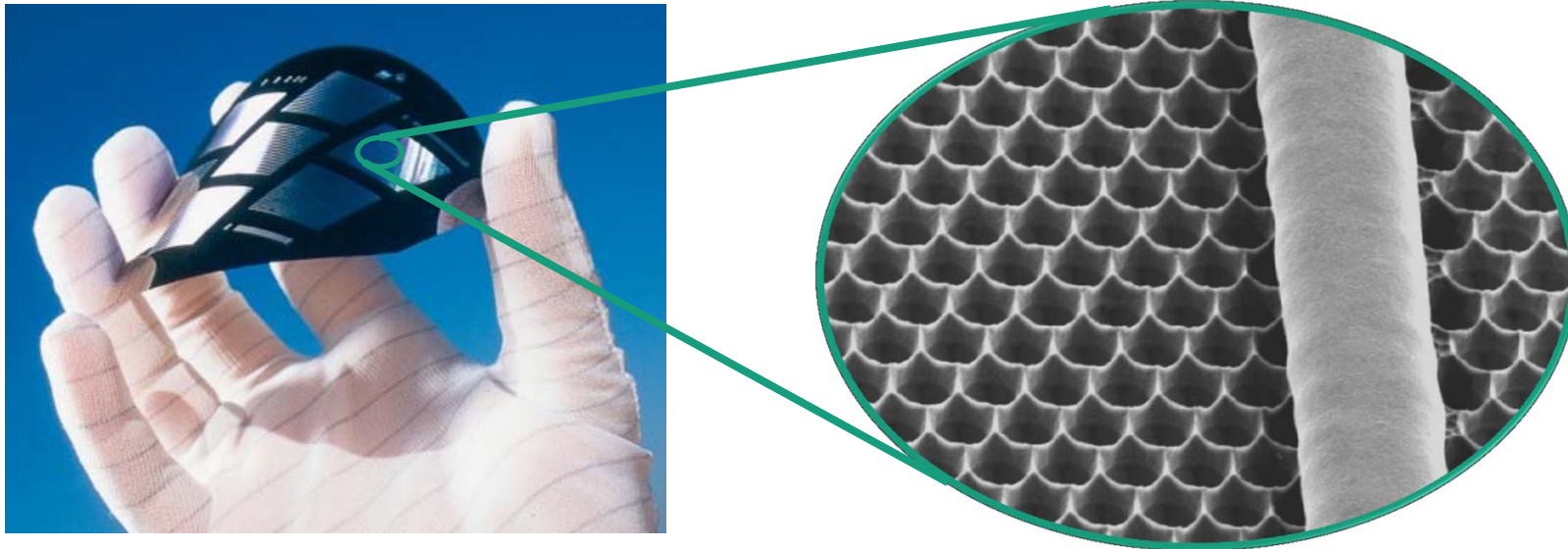


Nano-Fluidic Devices

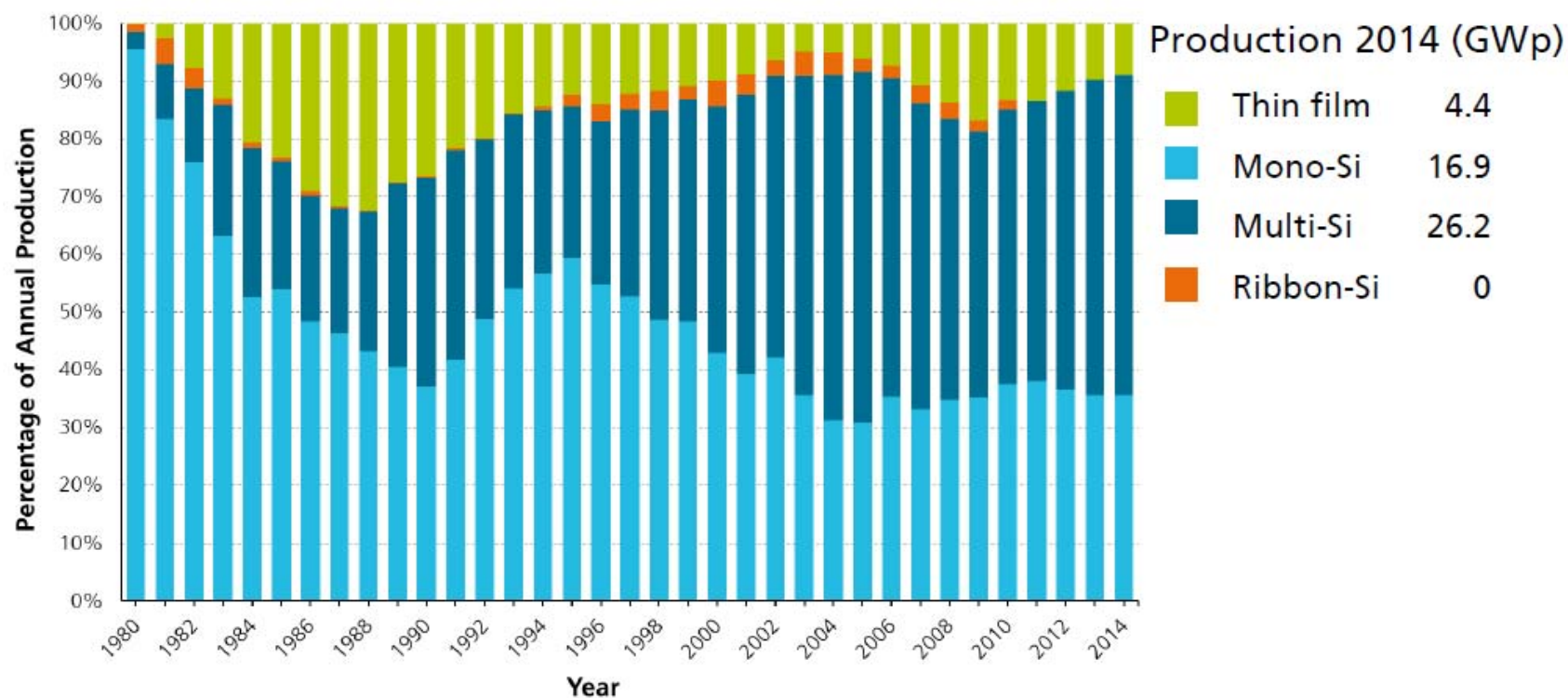


Photon Management Structures for Solar Cells

- Thin solar cells ↔ high quantum efficiencies
- Photon management structures of increasing importance for solar cells
- Challenge: cost effective production of very precise structures on large areas



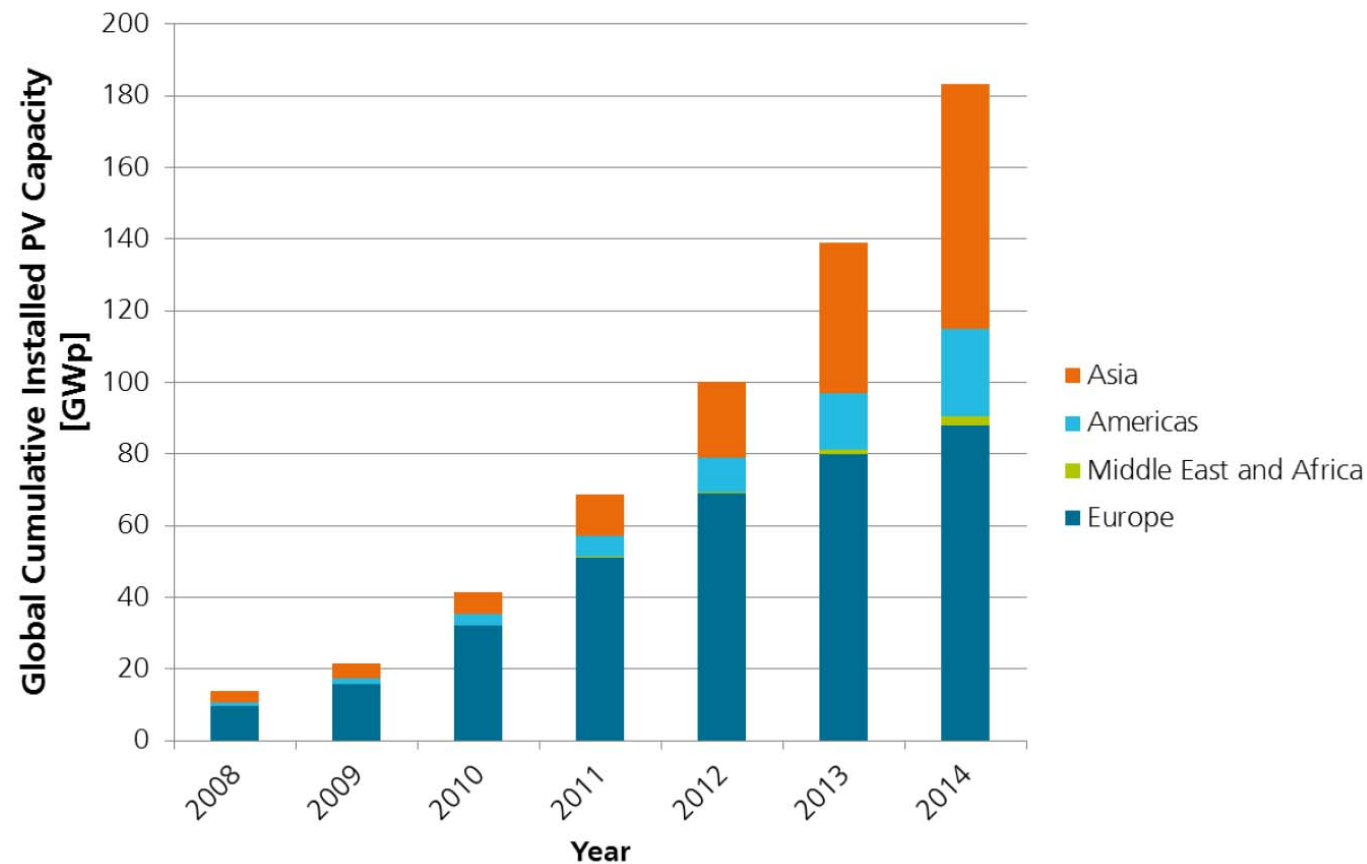
Facts and Trends – Technology Shares



Data: from 2000 to 2010: Navigant; from 2011: IHS (Mono-/Multi- proportion by Paula Mints). Graph: PSE AG 2015

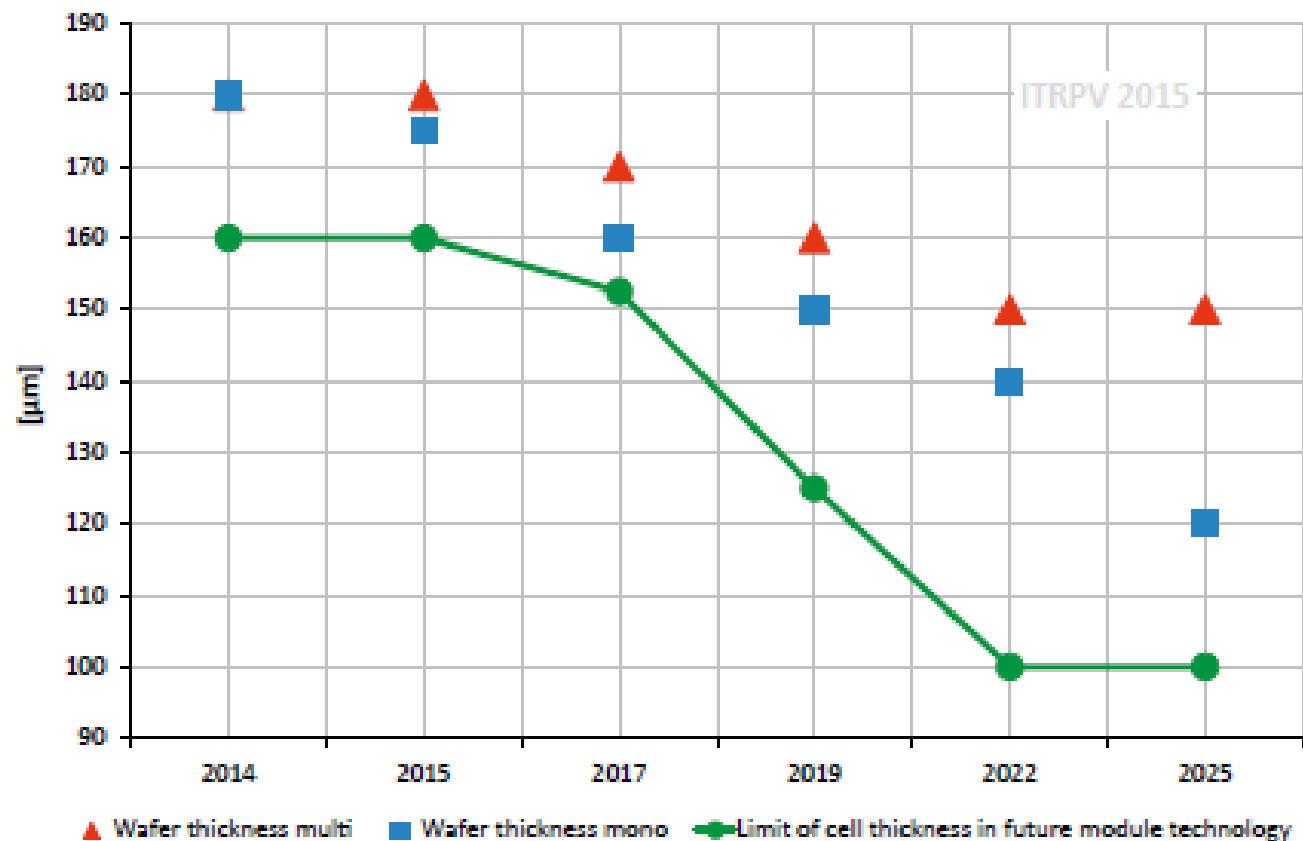
©Fraunhofer ISE: Photovoltaics Report, updated: 26 August 2015

Facts and Trends – Market Volume



©Fraunhofer ISE: Photovoltaics Report, updated: 26 August 2015

Facts and Trends – Wafer Thicknesses

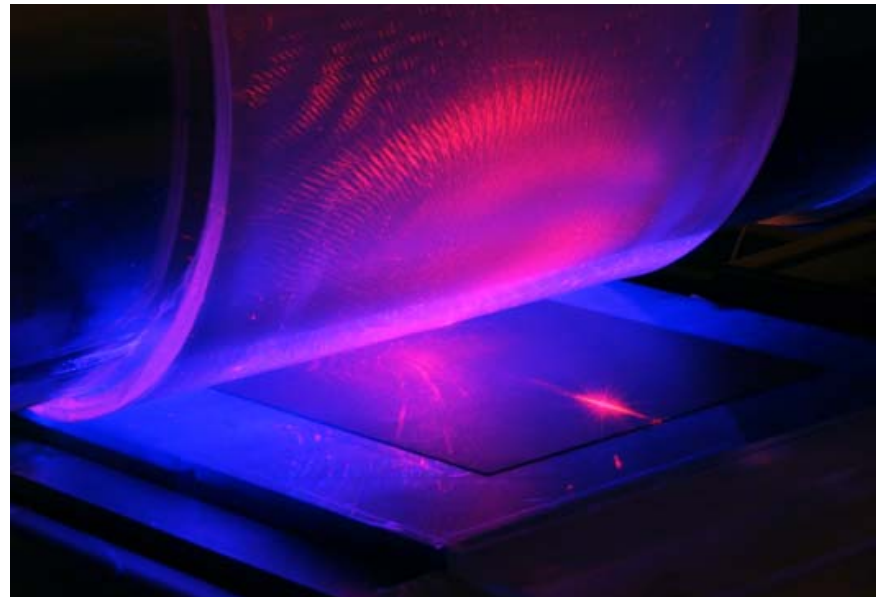


Quelle: ITRPV, Revision 1, July 2015

Nanoimprint Lithography - Roller-Tool

Replication of Photonic Structures

- UV-exposure throughout flexible stamp
- Imprinted area: 156 x 156 mm²
- Excellent adaptability to rough surfaces
- Homogeneous and low residual layer thickness (< 100 nm)
- Successfully tested on very thin wafer substrates (50 µm)

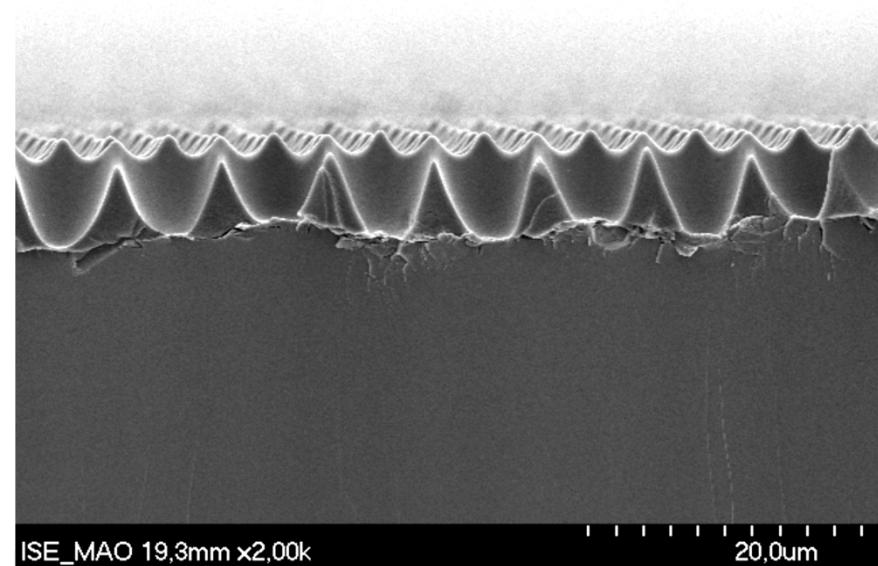


H. Hauser et al., IEEE Journal of Photovoltaics,
2 (2),114-122 (2012)

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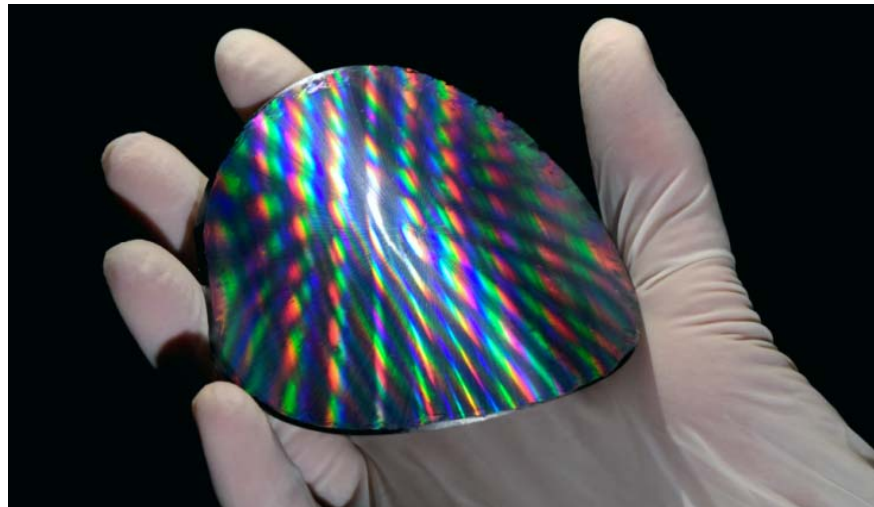


H. Hauser et al., IEEE Journal of Photovoltaics,
2 (2),114-122 (2012)

Nanoimprint Lithography - Roller-Tool

Replication of Photonic Structures

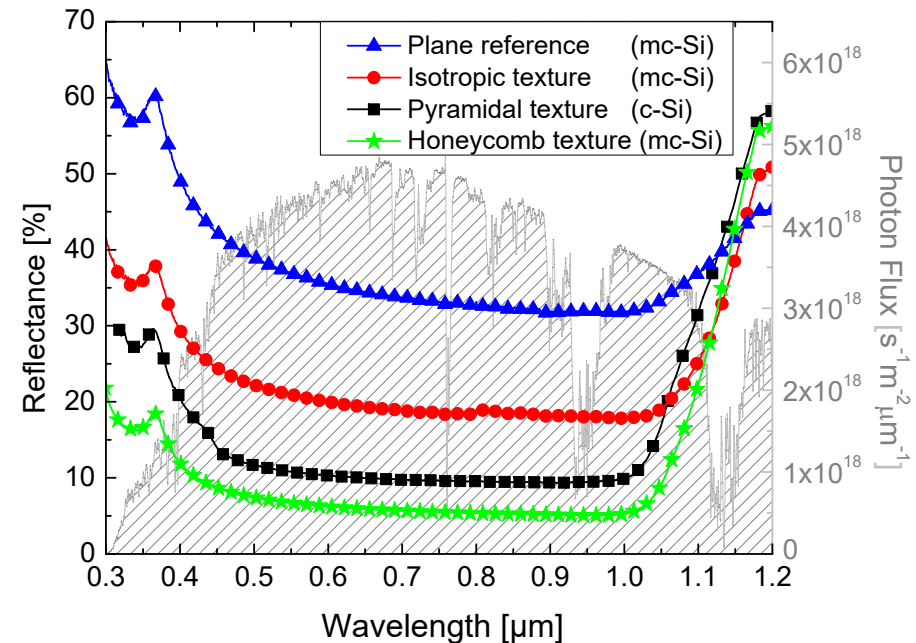
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H. Hauser et al., IEEE Journal of Photovoltaics,
2 (2),114-122 (2012)

Honeycomb Front Side Texture for Silicon Solar Cells

- Excellent optical performance even outperforming pyramidal textures (shown without ARC) [1]
- J_{sc} of 40.6 mA/cm² demonstrated on FZ material (2 x 2 cm²) [2]
- This corresponds to an optical efficiency η_{opt} of 87.5 % (electrons out / photons in)

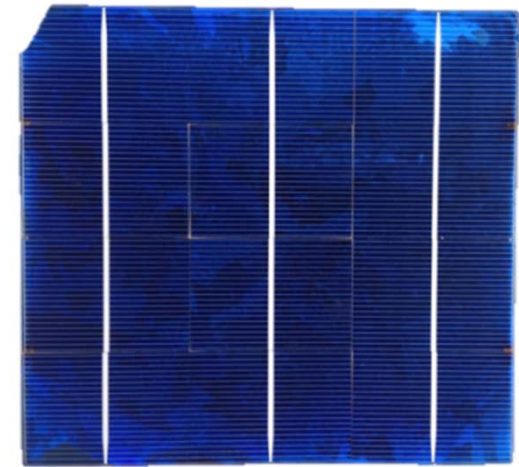


[1] A. K. Volk et al., accepted for publication in IEEE Journal of Photovoltaics, (2015)

[2] H. Hauser et al., IEEE Journal of Photovoltaics, 2(2), 114–122 (2012).

Honeycomb Front Side Texture for Silicon Solar Cells

- Al-BSF Solar Cells
 - 156 x 156 mm²
 - Standard ARC
 - In-line capable texturing
 - Screen printed metallization



■ Best Cell Results [1]

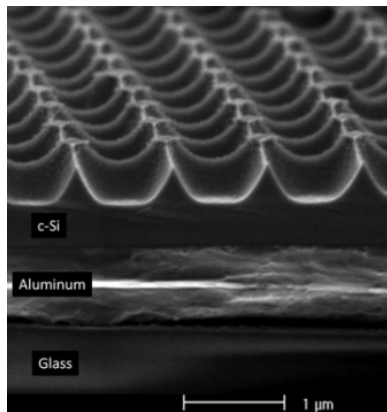
	V _{oc} [mV]	J _{sc} [mA/cm ²]	FF [%]	η [%]
ISO-Texture Cell	618.3	35.0	79.3	17.3
HC-Texture Cell	618.4	36.2	79.5	17.8
HC-Texture Cell (5 x 5cm ²)	620.0	37.5	76.7	17.9

[1] A. Volk et al, IEEE Journal of Photovoltaics, 99, 1-7 (2015)

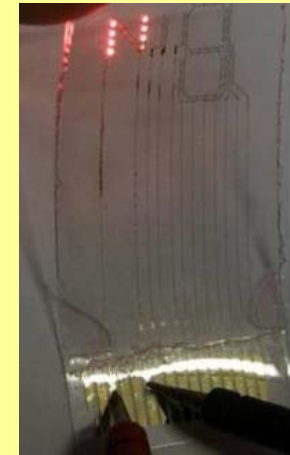
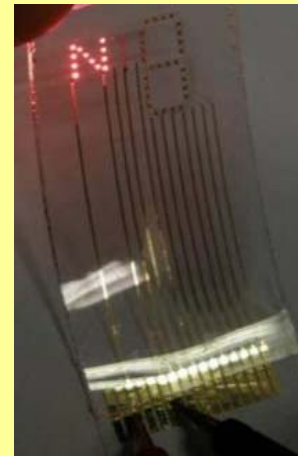
ISO=isotropically etched, HC = honeycomb, ARC = antireflexion, BSF=Back surface field

Nanopatterning – Main NIL Applications

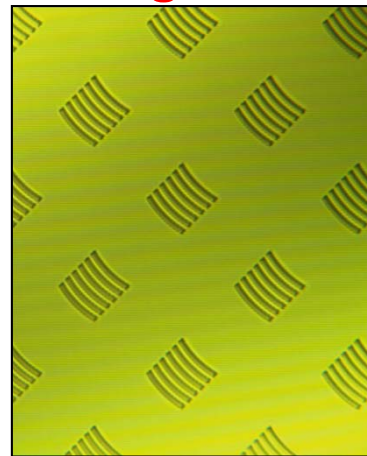
Photovoltaics



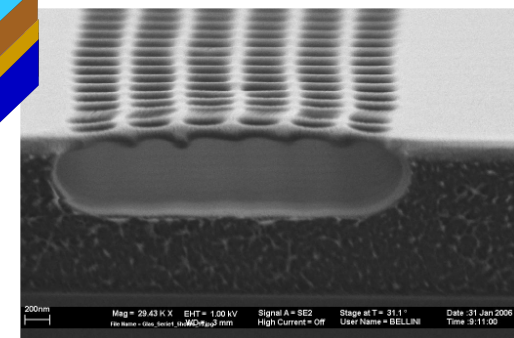
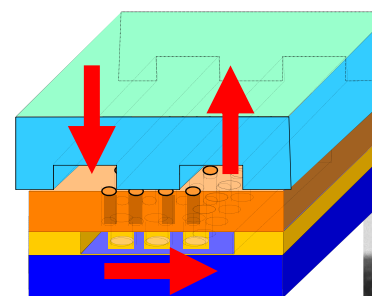
Transparent electrodes



Backlight Display Waveguide



Nano-Fluidic Devices



NIL for Transparent Electrodes

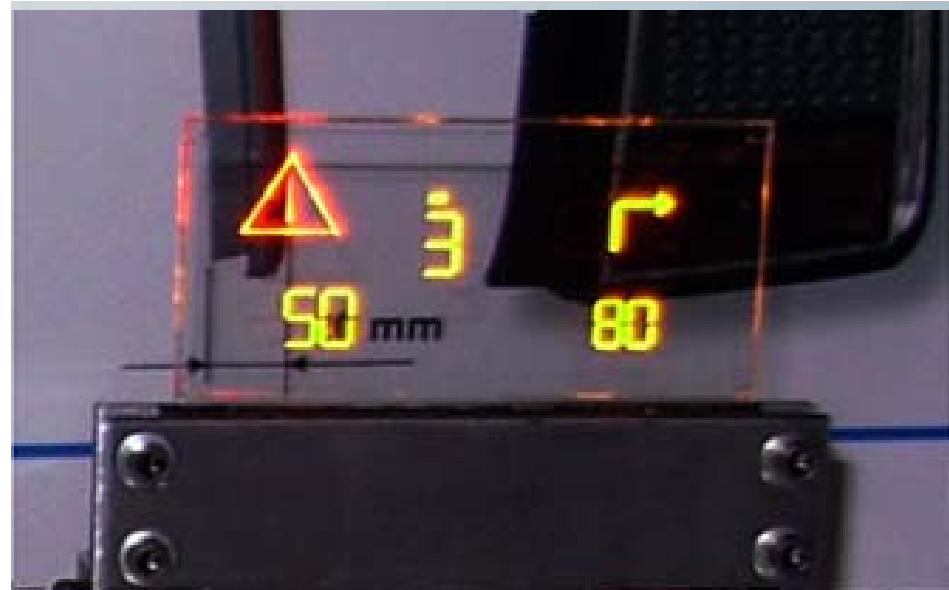
Head-up Displays integrating an emissive array of LED dice onto a transparent substrate unlike conventional HUD, which are virtual, in the emissive HUD the emitting layer is integrated into the transparent substrate.

Advantages of eHUD

- **Installation volume required**
<100ml (standard HUD 3-4 liters)
- **High luminance:** >5000cd/m²
- **Potentially low cost:** <30% standard HUD
- **Image:** real, monochrome or multi-color,

CURRENT LIMITATIONS

- **High resistivity TCOs** (>10 Ohm square for a 100nm ITO film) with limitation on the layout of the display
- **Light reflection on windshield and pixeled information** (interference with primary driving task, not clear images)
- **Substrate costs**

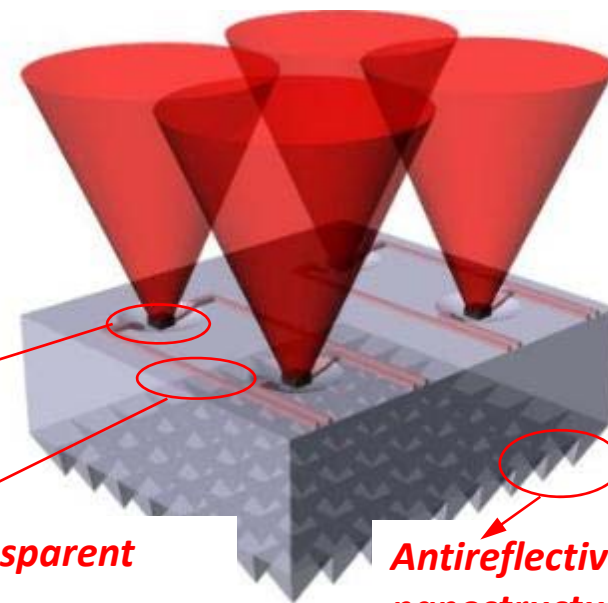


emissive HUD with integrated diodes

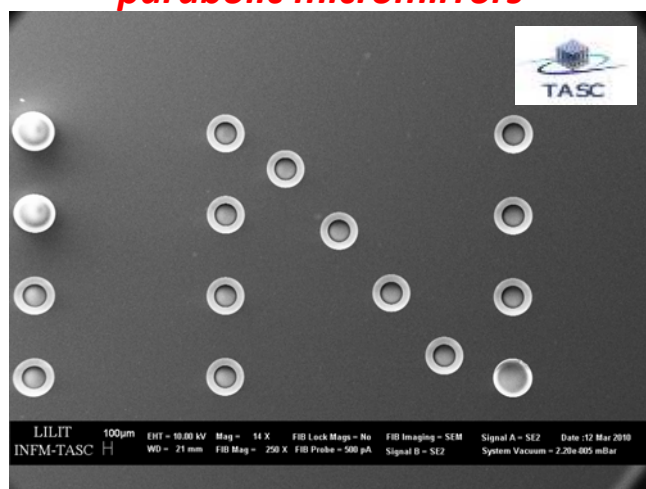
NIL for Transparent Electrodes

NAPANIL IMPROVEMENTS

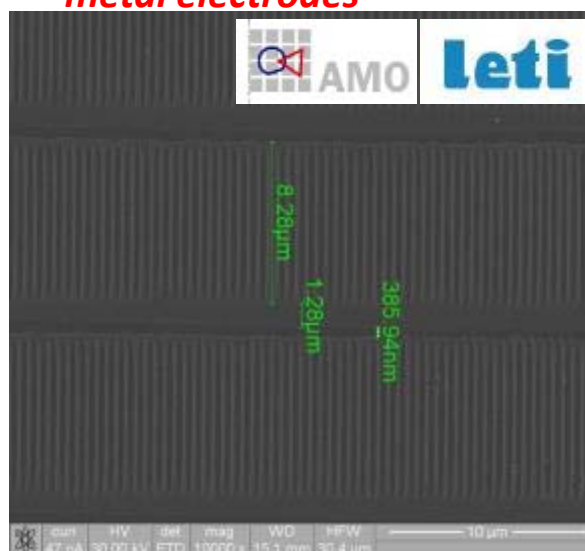
- Increased transparency of conductive wires
- Lower operative voltage and power consumption
- Flexible substrates
- Increased optical performances (antireflection, light control) with enhanced safety and comfort
- Low cost processes



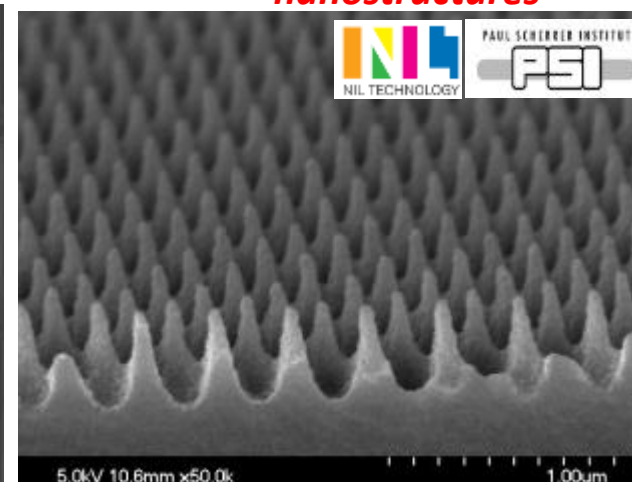
3D micropatterning of parabolic micromirrors



Nanopatterning of transparent metal electrodes

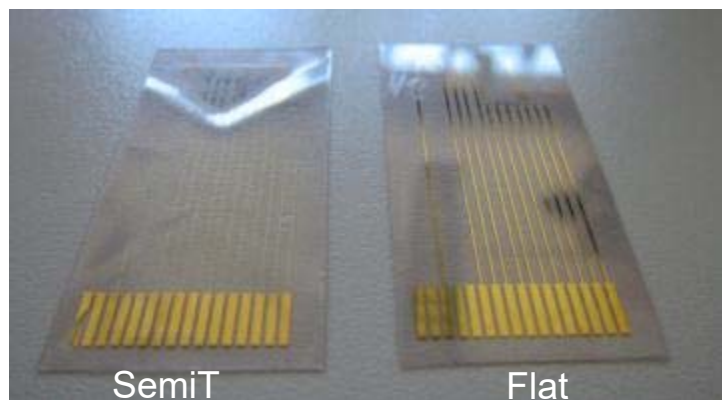


Antireflective nanostructures

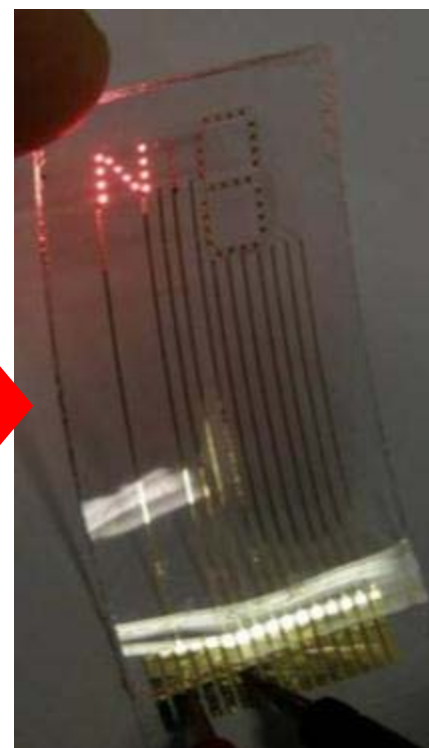
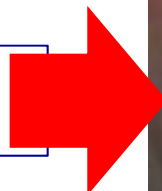


NIL for Transparent Electrodes

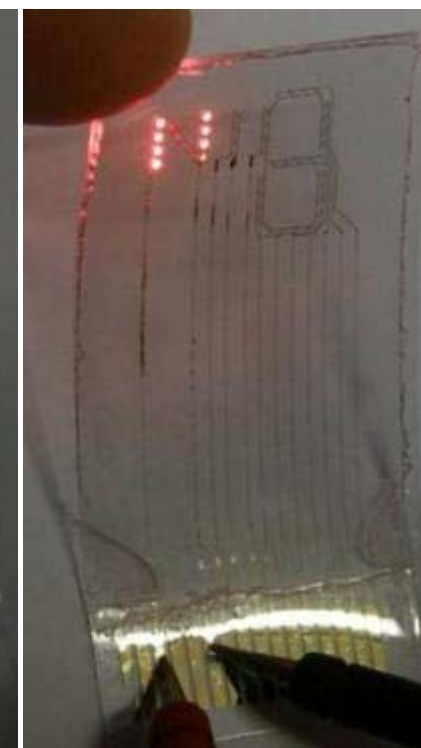
eHUD prototype integrating double side patterned plastic substrate



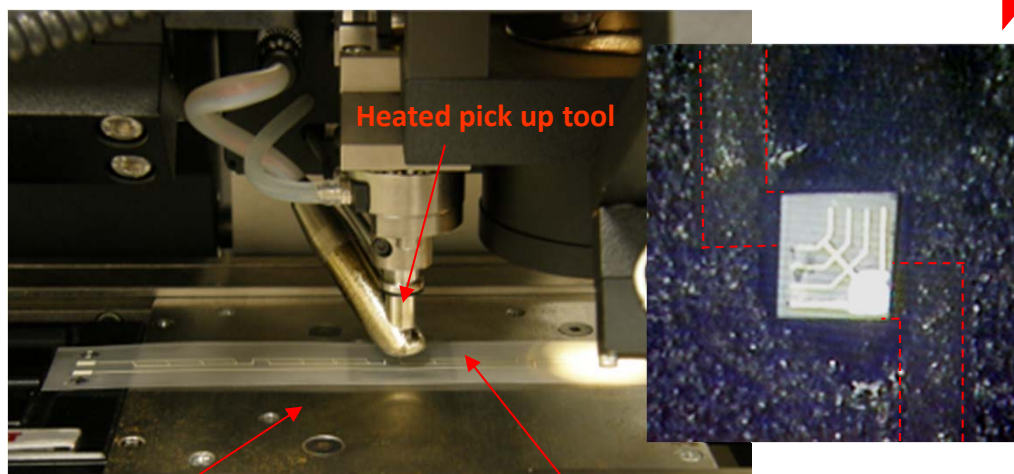
LEDs bonding optimization using
flip-chip technology



Flat



SemiT



Heated bottom plate

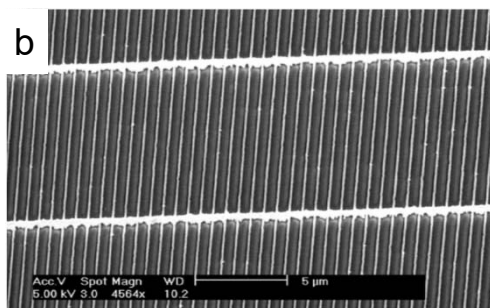
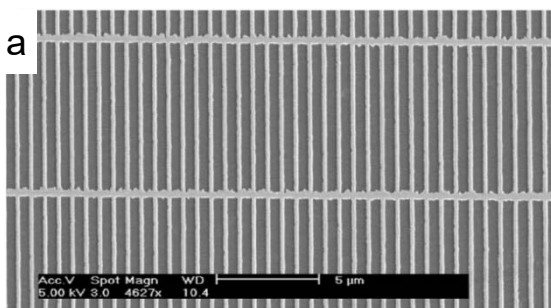
Substrate

NIL for Transparent Electrodes

eHUD prototype integrating double side patterned plastic substrate



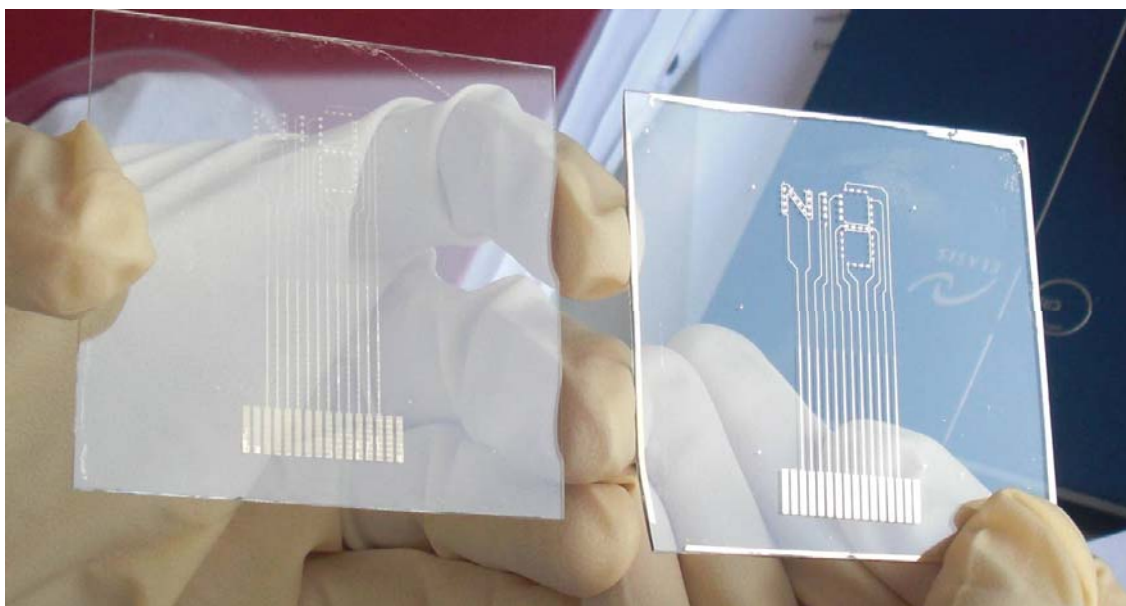
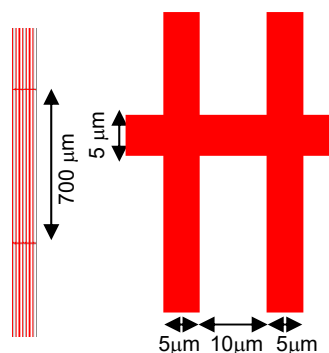
State of the art



Nanoimprinted semitransparent Metal Electrodes and their application in organic light-emitting diodes

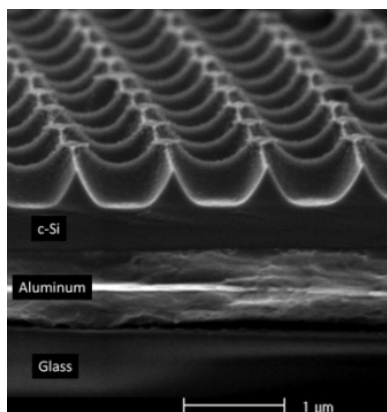
Myung-Gyu Kang and L. Jay Guo, Adv. Mater. 2007, 19, 1391–1396

It also works with micrometer sized semi-transparent tracks

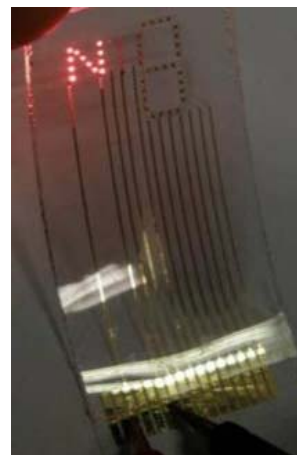


Nanopatterning – Main NIL Applications

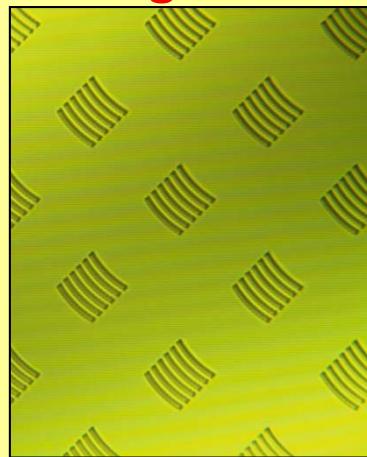
Photovoltaics



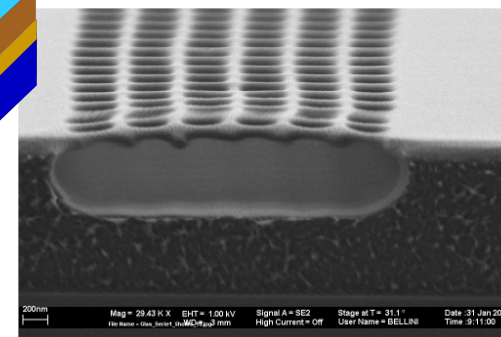
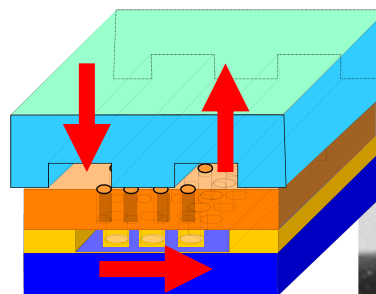
Transparent electrodes



Backlight Display Waveguide



Nano-Fluidic Devices

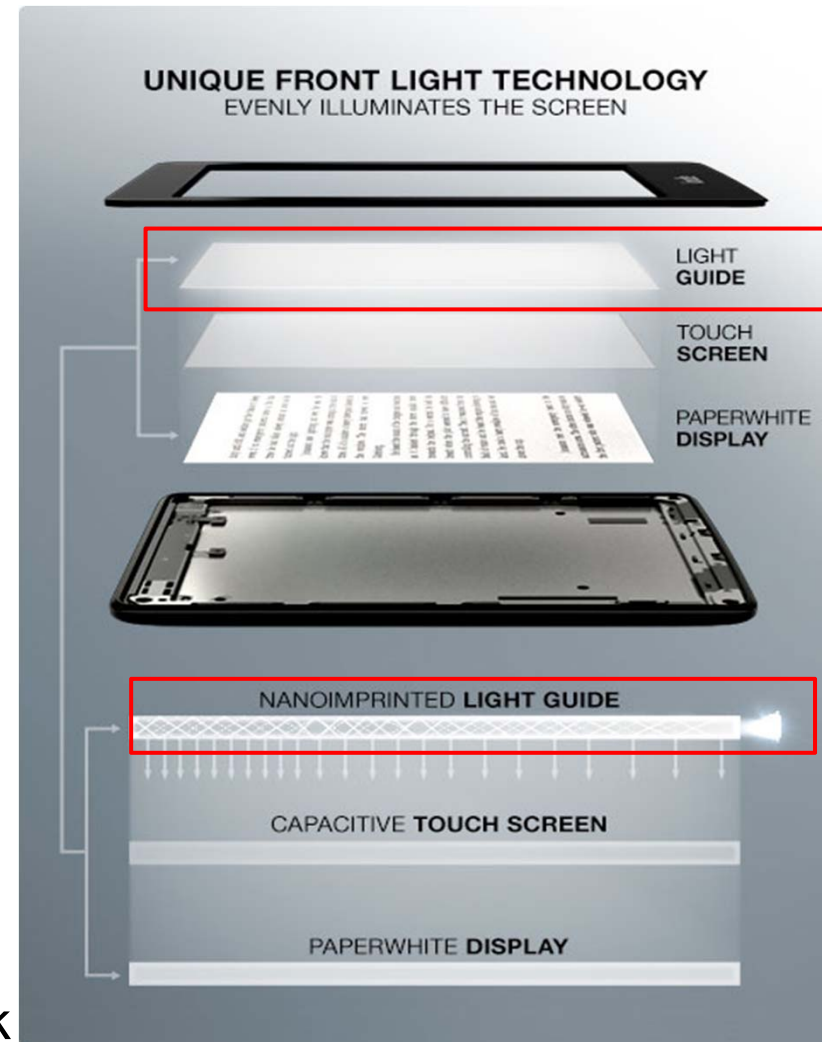


Manufacturing of Displays with integrated Illumination



But: e-paper displays do not have backlight illumination

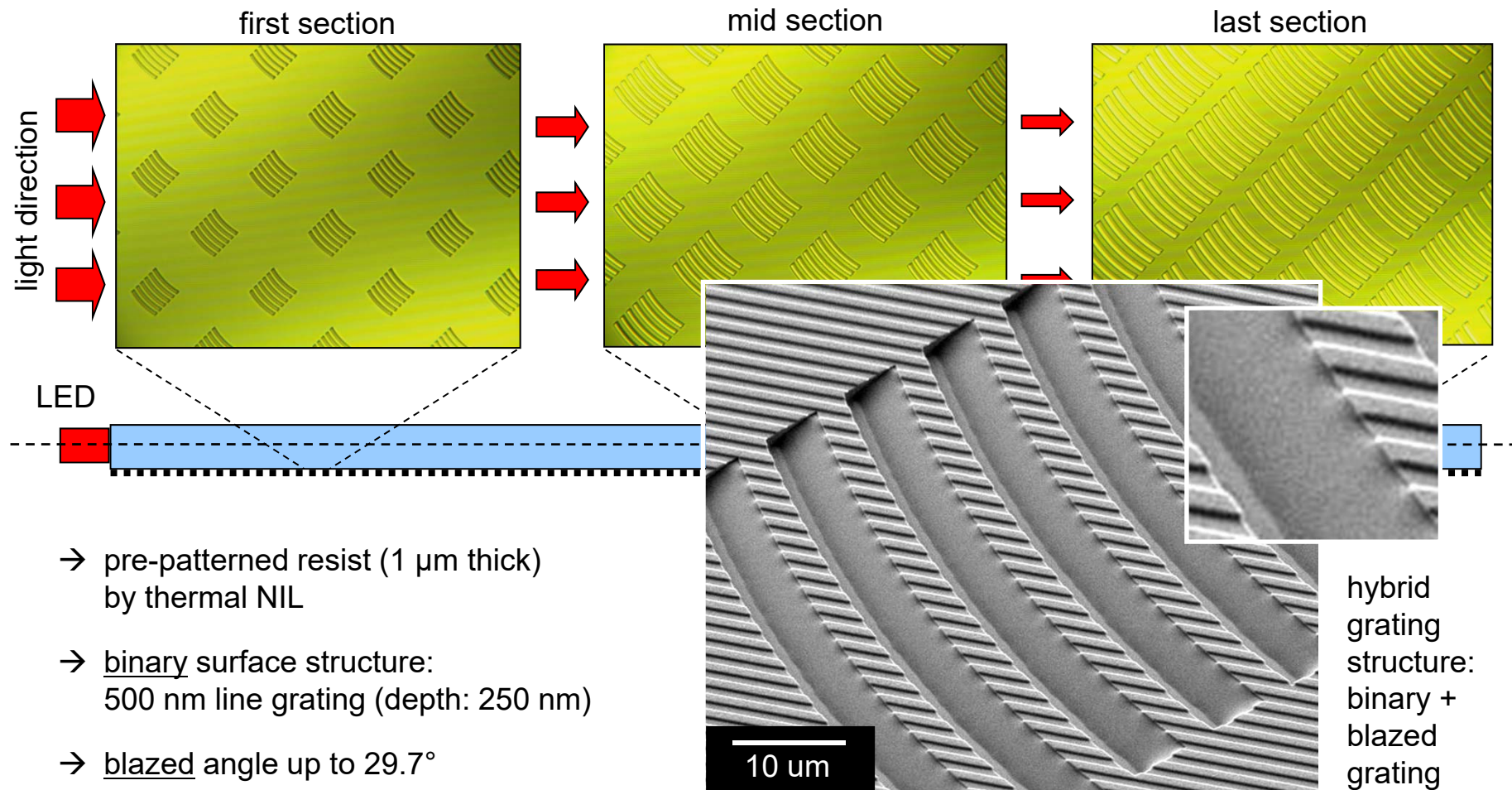
Solution: illumination with frontlight, with light coming from top side onto e-ink



<http://www.amazon.com/dp/B007OZO03M>

Fabrication of hybrid gratings by selective thermal reflow

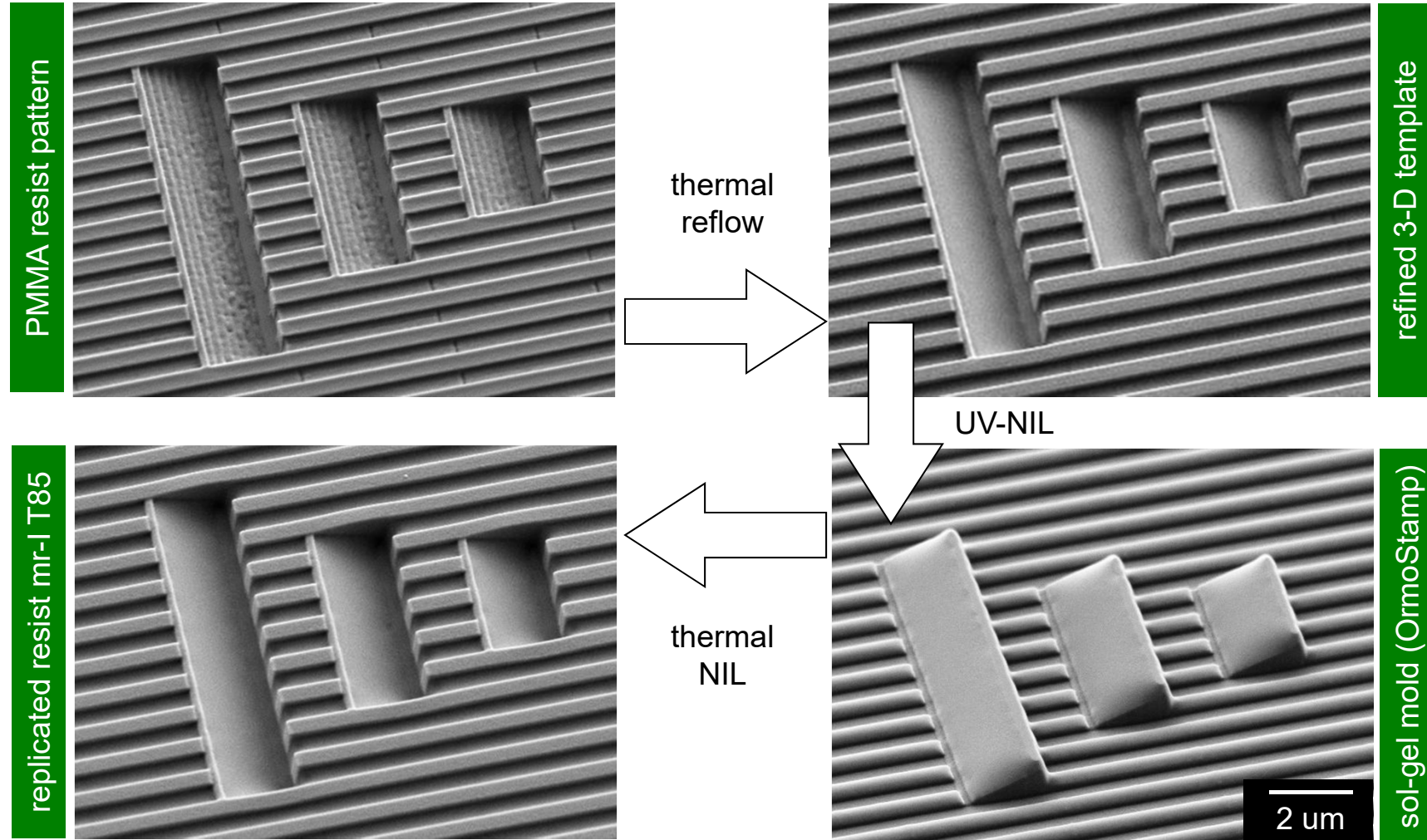
Pixelized lightguide surface for backlighting devices: outcoupling elements and anti reflective pattern



Kari Rinko, Light outcoupling structure for a lighting device, Patent application: US 2008/0225393 A1

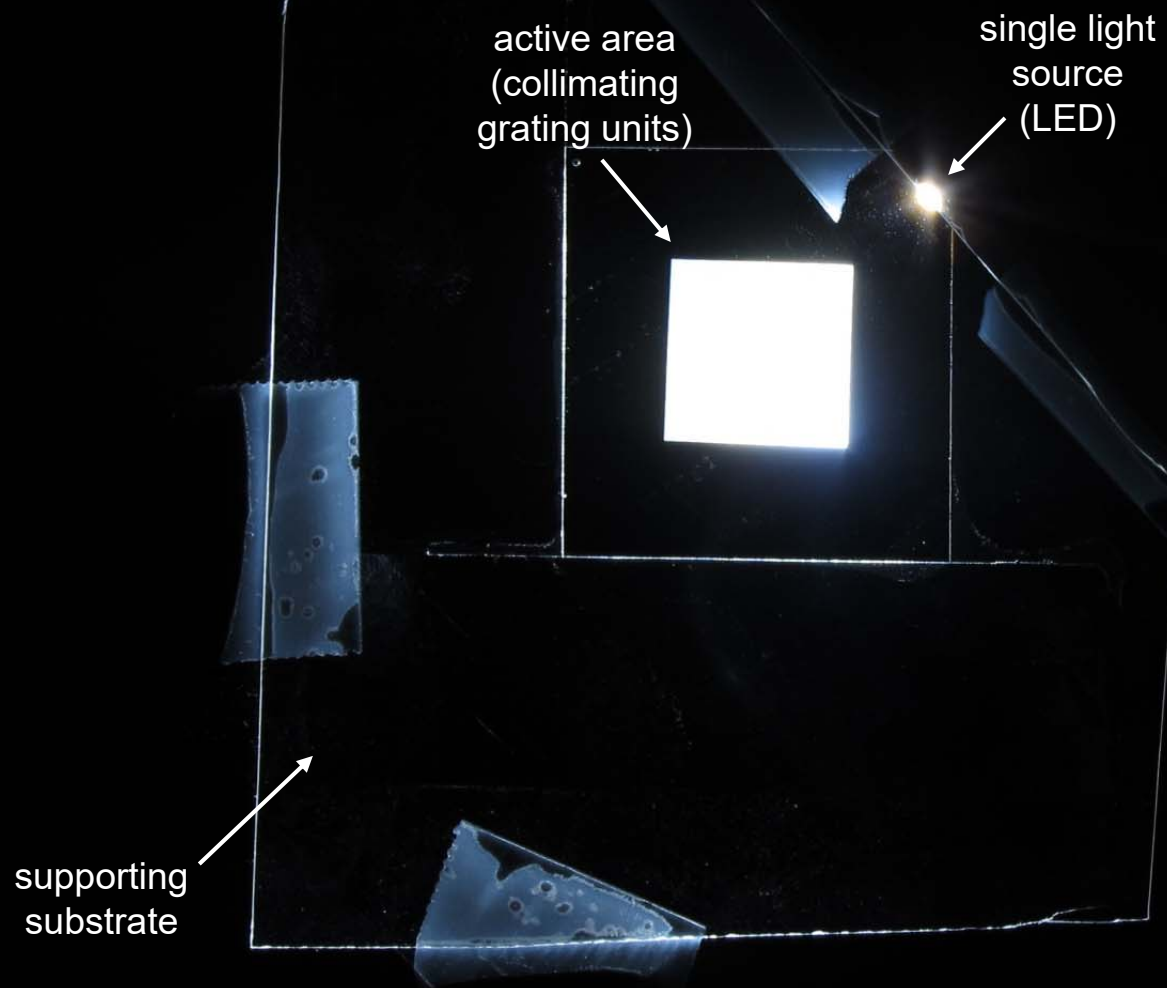
Fabrication of hybrid gratings by selective thermal reflow

3-D pattern are copied into a sol-gel material and repeatedly replicated into a polymer resist



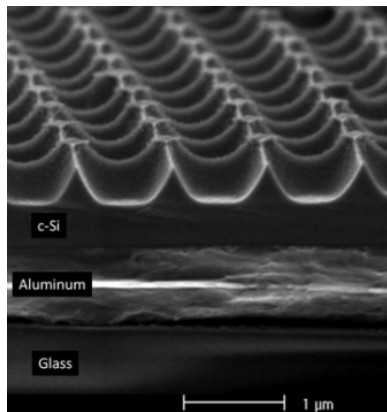
Optical appearance of the backlighting test device

Performance of active area with 74.000 outcoupling elements with varying density and orientation

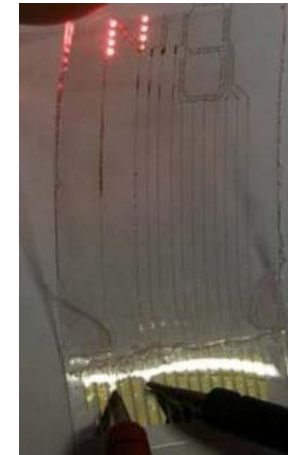


Nanopatterning – Main NIL Applications

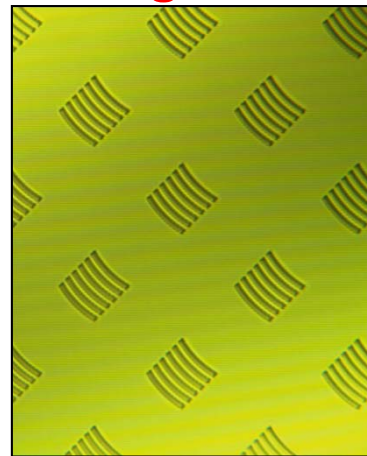
Photovoltaics



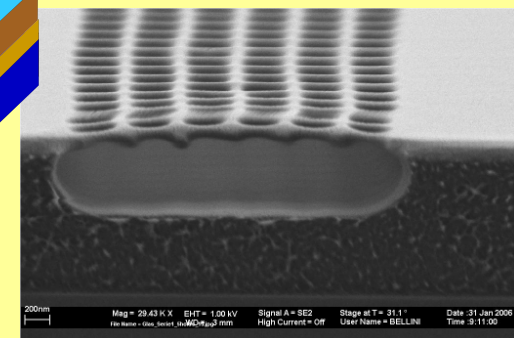
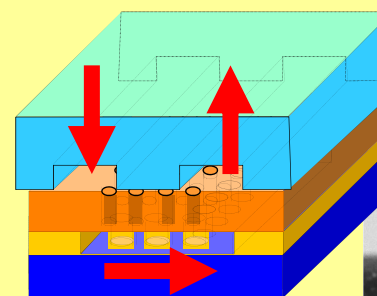
Transparent electrodes



Backlight Display Waveguide



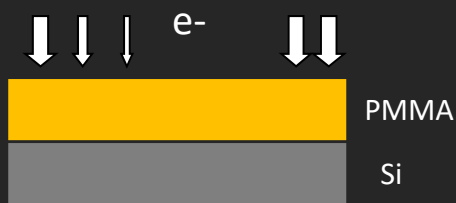
Nano-Fluidic Devices



Fabrication processes for nanofluidics

LIGA + NIL: Grey scale EBL + THERMAL REFLOW

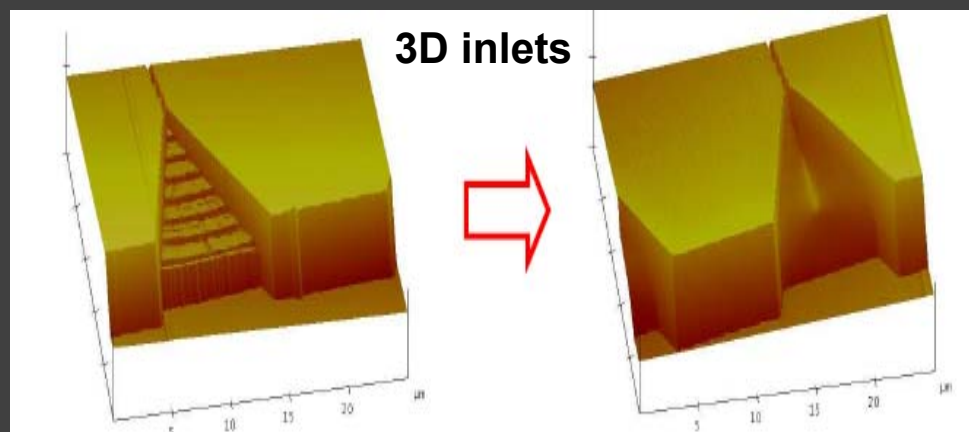
e-beam exposure



Development



Thermal reflow: $T \sim T_g$



FIB

Grey scale EBL + thermal reflow

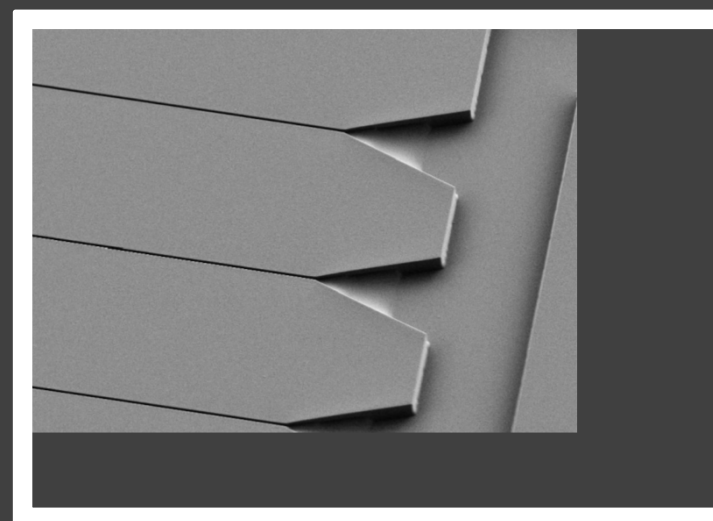
Funnel from

□ 1 μm to

□ 20 nm

channel

- Ultra smooth structures
- No steps
- High reproducibility
- High throughput

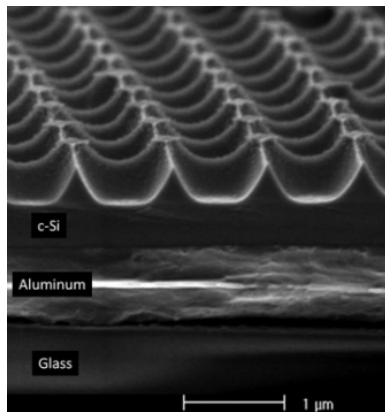


16/08/2016

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Nanopatterning – Main NIL Applications

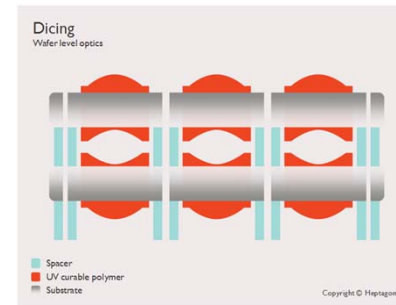
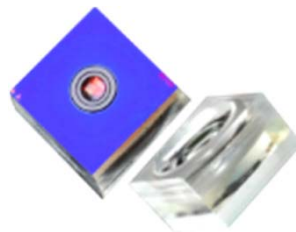
Photovoltaics



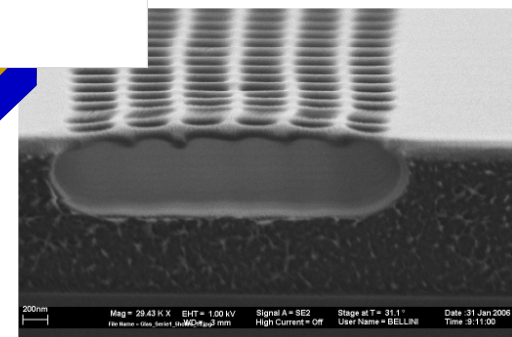
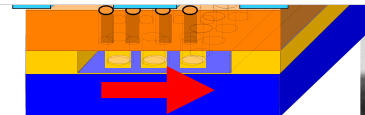
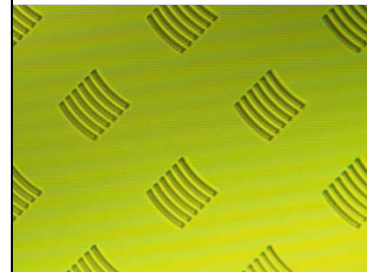
Transparent electrodes



Micro-optical systems



Backlight Display

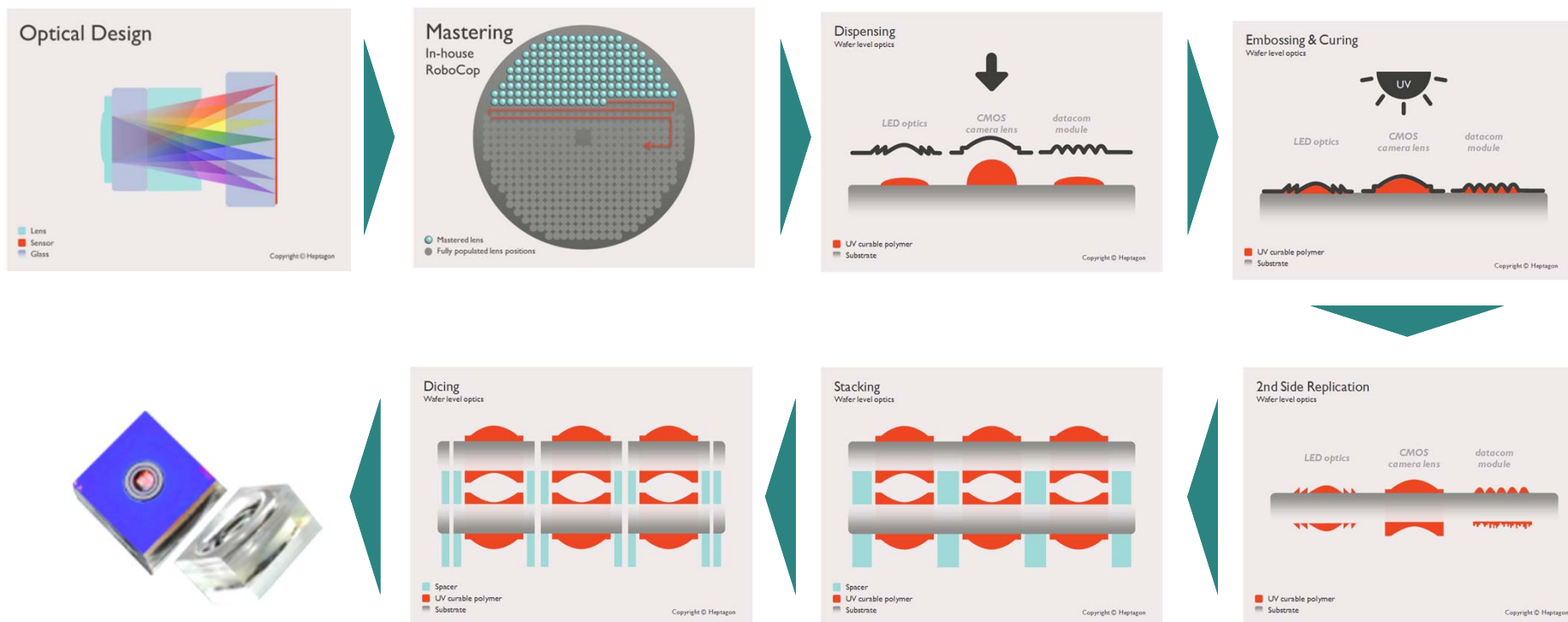


ces

HEPTAGON microsystems in smart devices



UV Replication Process



NOTE: Most of the lenses are still «micro», but the techniques are ready to be adapted to nanopatterning

Wafer Level UV Replication Technology

Micro Optics

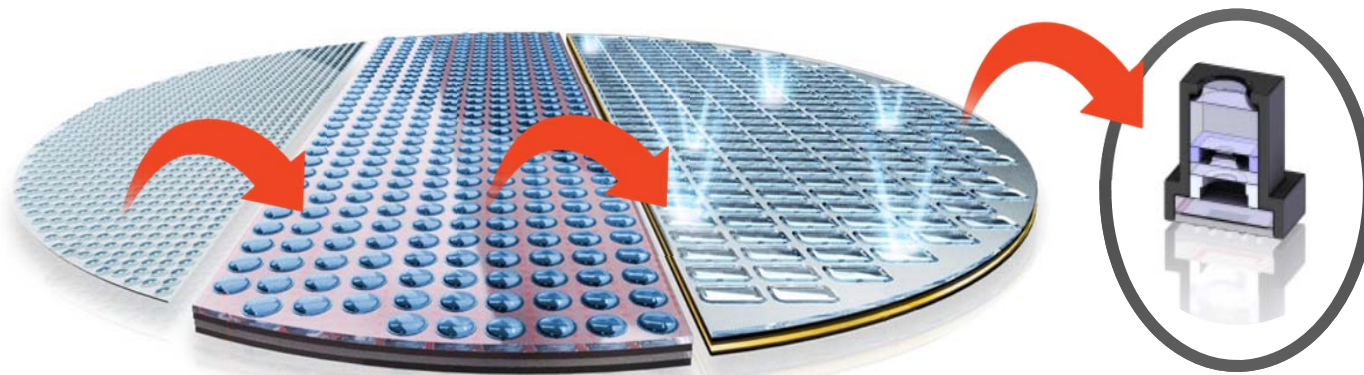
- Precision stacking
- Spacer technology
- Advanced packaging technologies

Micro Modules

- Non imaging modules
- New advanced packaging methods
- Reconstructed PCBs
- Electronics

Imaging Solutions

- Miniatureized camera technology
- 3D Systems
- ToF sensor technology
- 3D software



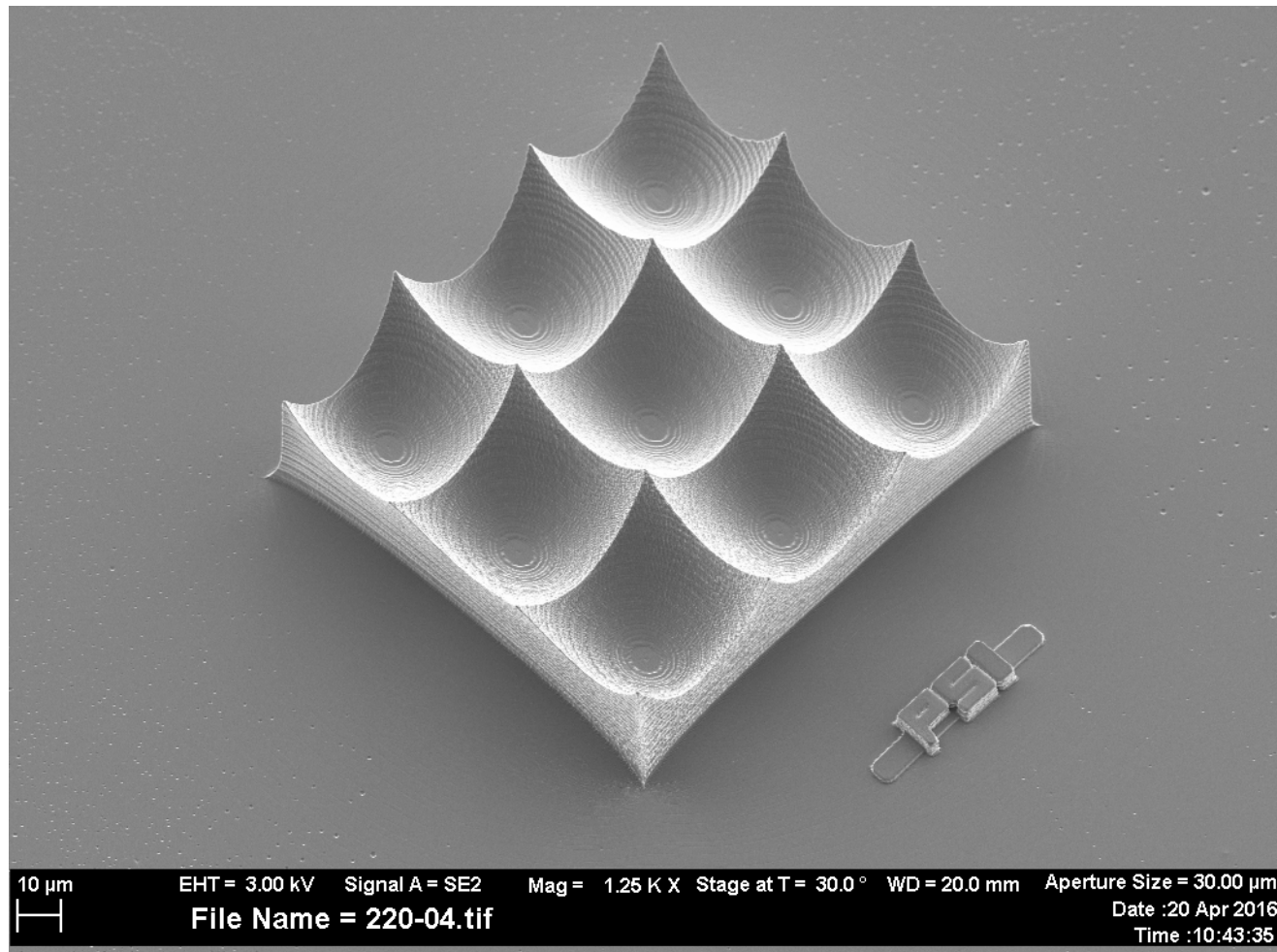
WLO
Wafer Level Optics

WLP
Wafer Level Packaging

WLI
Wafer Level Integration

WLM
Wafer Level Modules

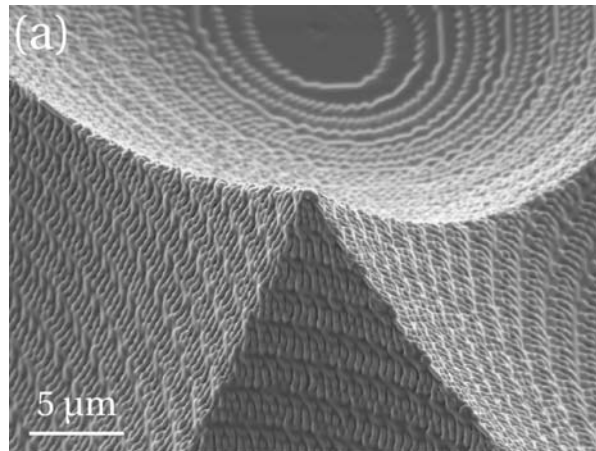
Surfaces of microstructures are typically «rough» in different dimensions



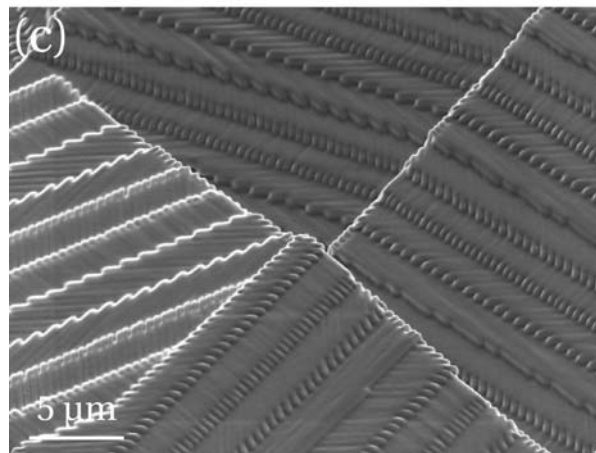
Test structure: Micro-lens array (3x3) concave 50 μm x 50 μm x 50 μm (each)

Distinction between structural details and unwanted «nano»roughness

Rough surface



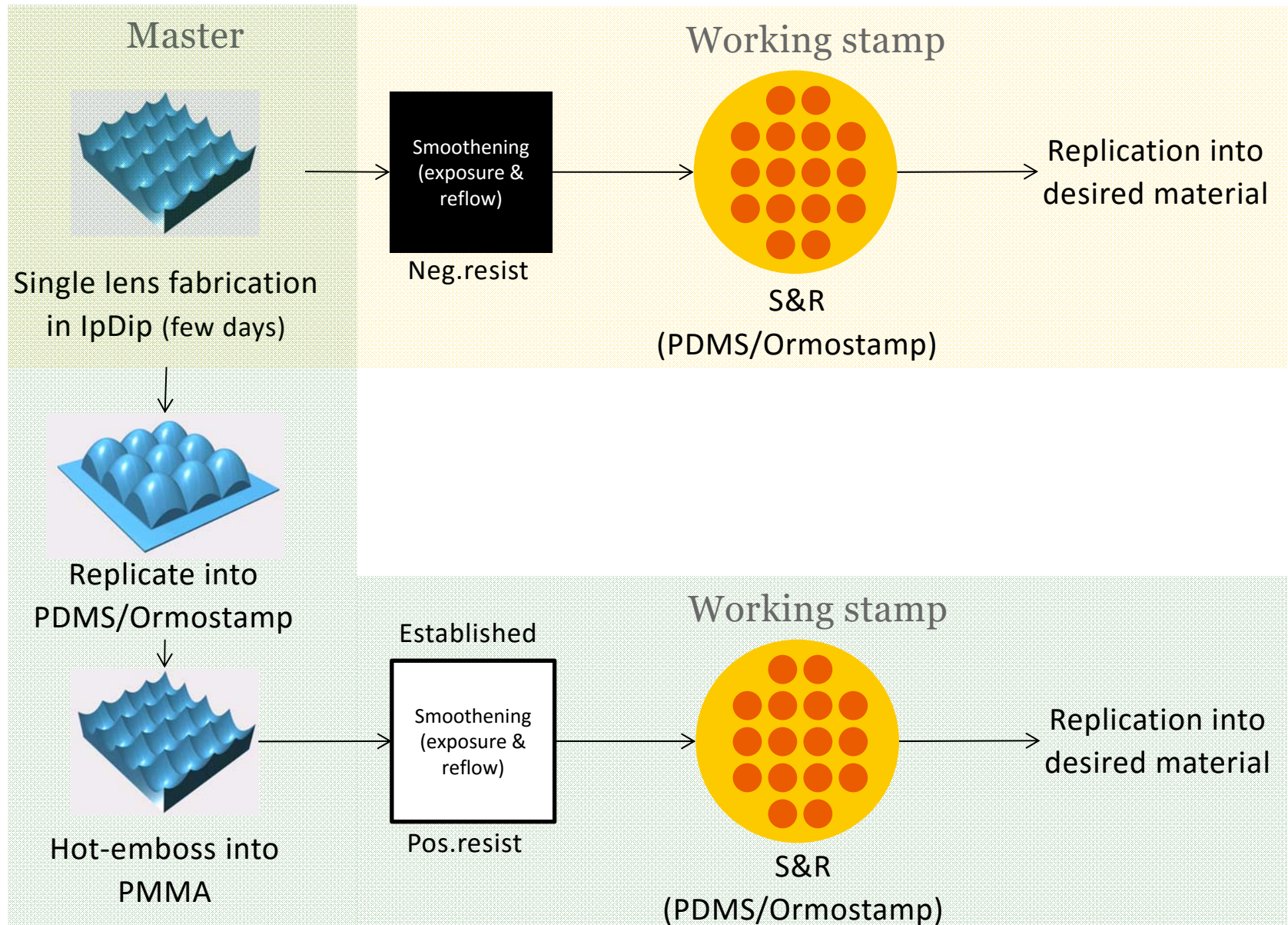
Concave
lenses



Tiled
slopes

Segments intersection: sharp $<1\ \mu\text{m}$ tips («high aspect ratio»)

Process flow with NanoScribe MLA



Micro lens array

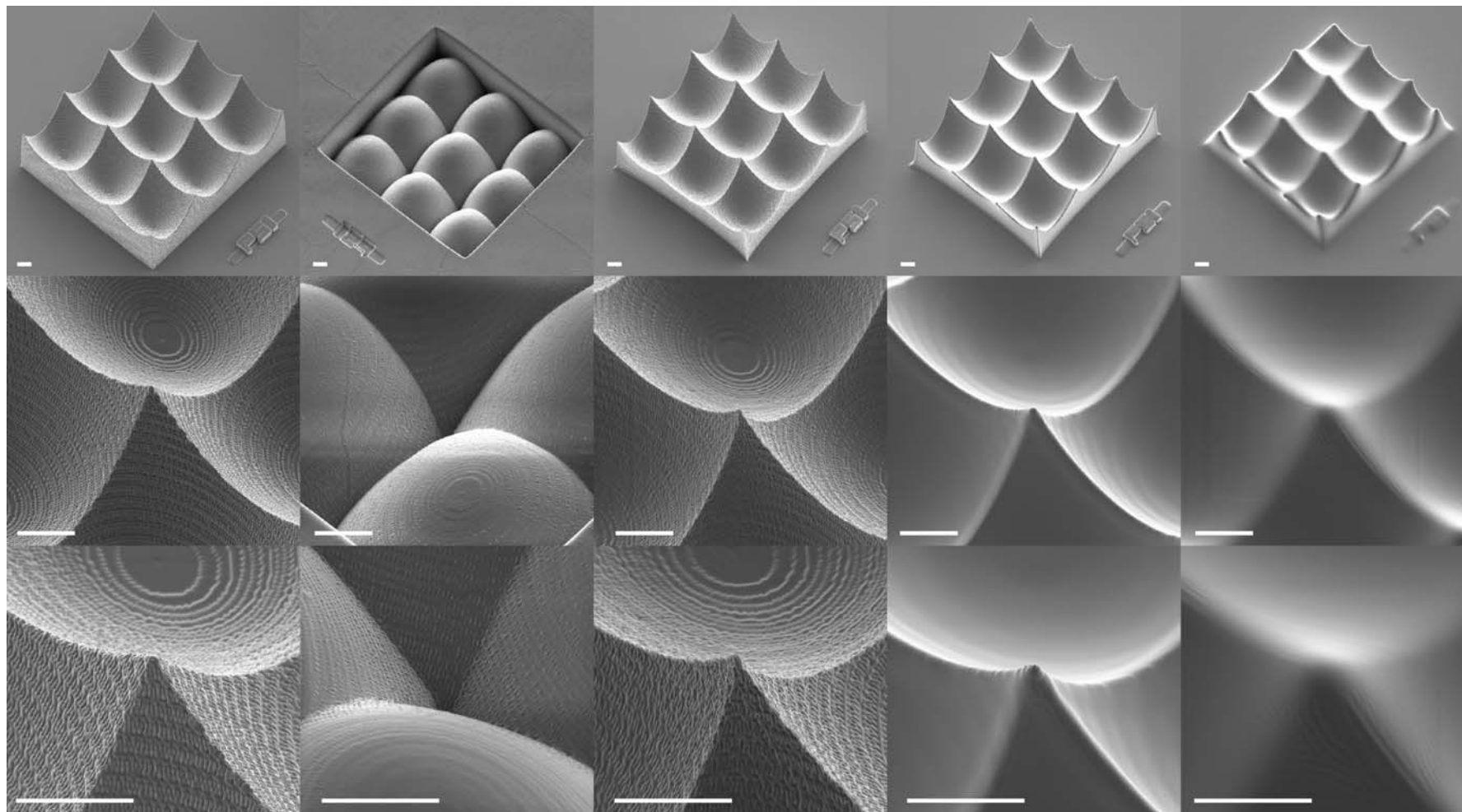
IpDip

UV PDMS

PMMA

Reflow (exp)

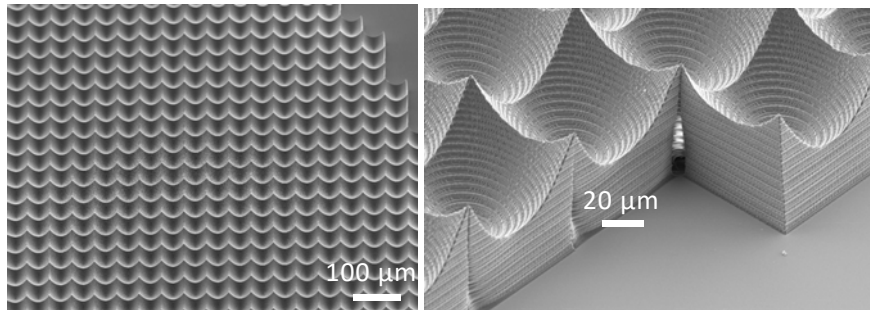
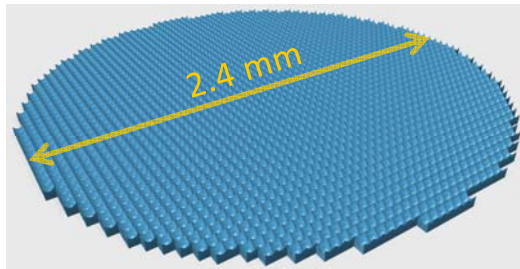
Reflow (no exp)



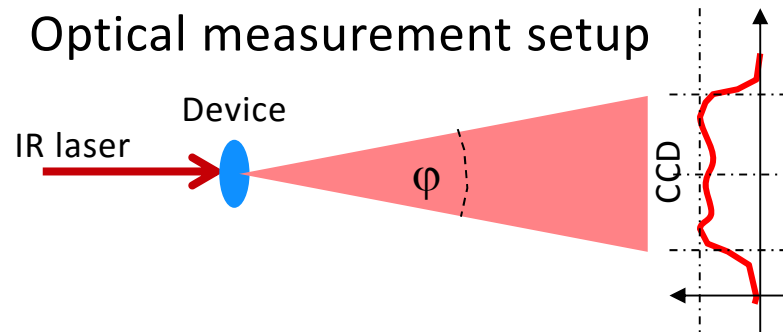
Scale = 10 μm

Device (48 hours writing)

Master fabrication

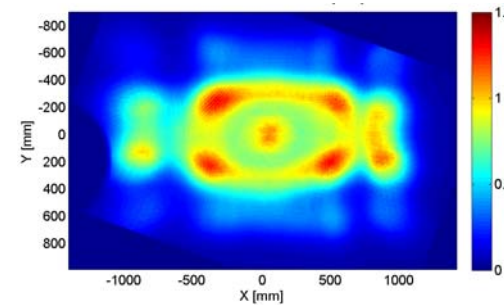


Optical measurement setup



FOI: Field of illumination given by angle ϕ_x

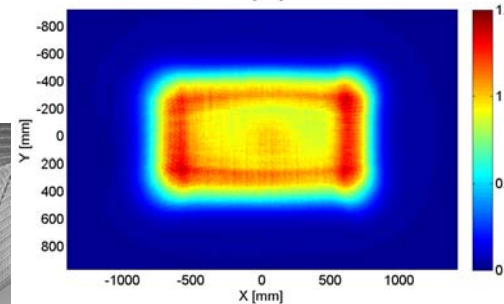
Intensity variation: standard deviation by Sigma



IpDip Master

x-FOI (75%) = 61.5°

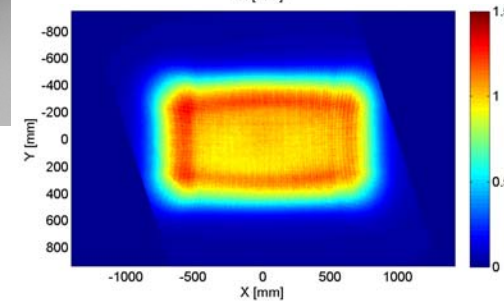
Sigma = 10%



PMMA as embossed

x-FOI (75%) = 75°

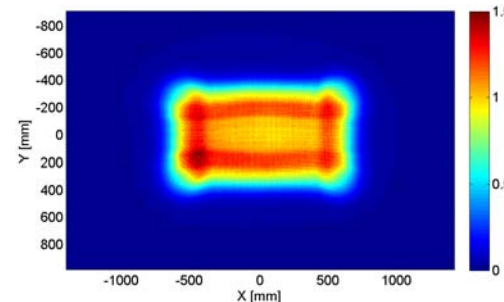
Sigma = 10%



PMMA exp+reflow

x-FOI (75%) = 74.5°

Sigma = 5%

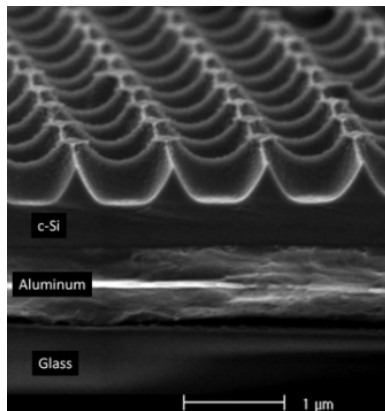


PMMA no exp reflow

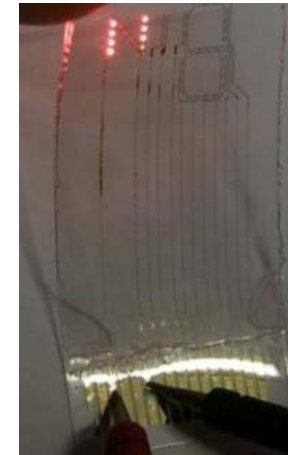
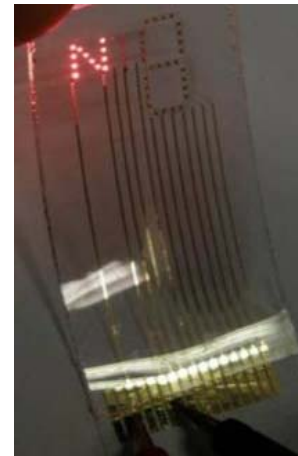
x-FOI (75%) = 63.2°

Sigma = 7%

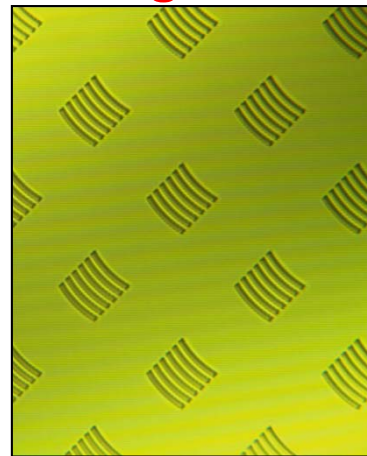
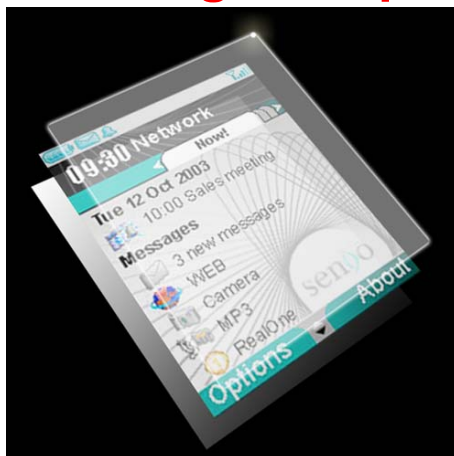
Photovoltaics



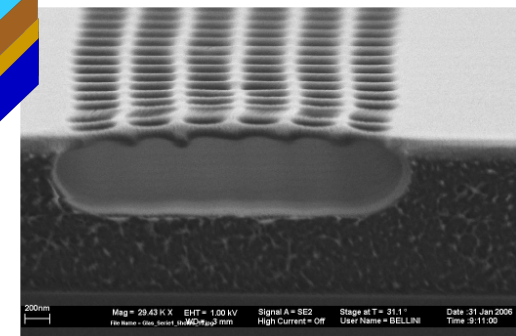
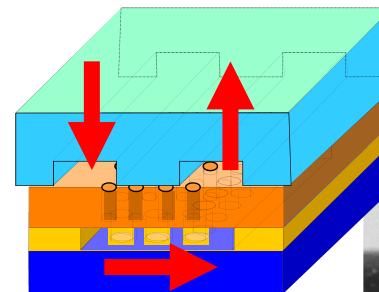
Transparent electrodes



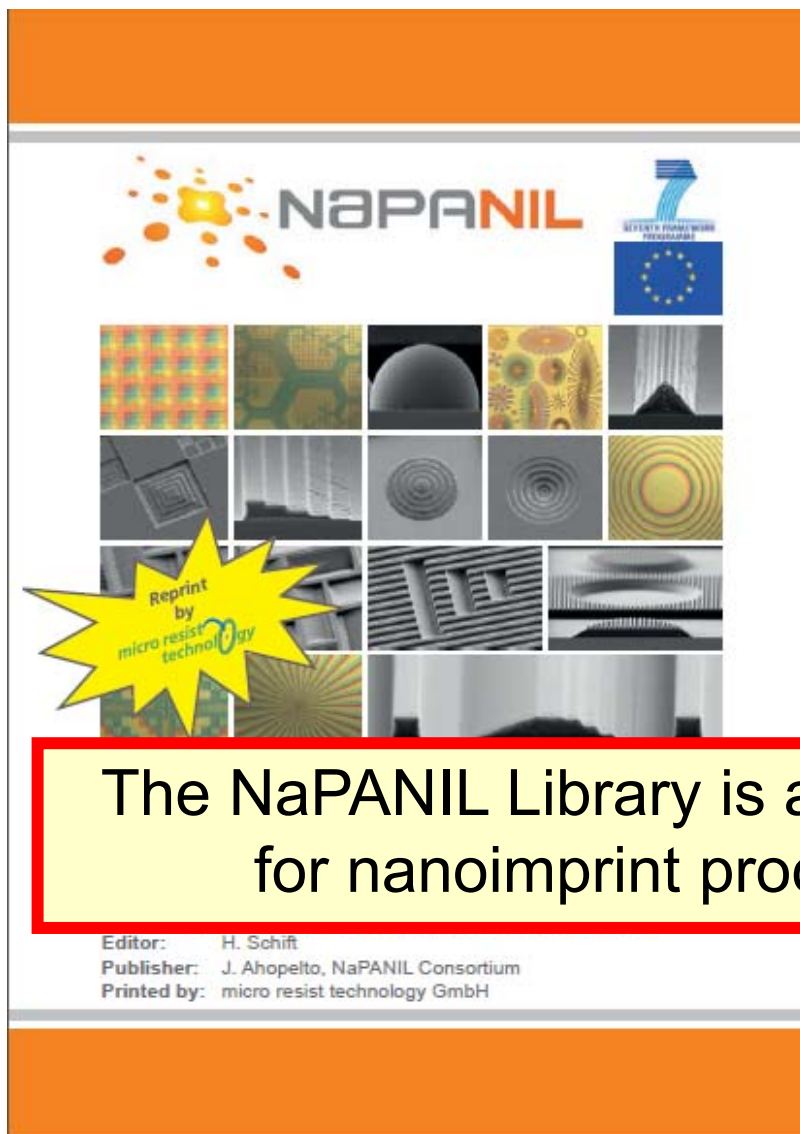
Backlight Display Waveguide



Nano-Fluidic Devices



NaPa Library of Processes: A Guide to Nanopatterning



NaPa Library of Processes				
NaPa				
Patterning Process	Patterning Scheme	Process	Specific advantages	Industrial Activity
Thermal Nanoimprint Lithography (NIL, T-NIL) – Hot Embossing Lithography (HEL)		Resist: hard, opaque (silicon wafers) Process: Thermoplastic molding at elevated temperature (100-200°C), demolding at low temperature (50-100°C) Tool: Hot presses (1-100 kN)	Similar to standard lithography (generating a thickness contrast of a resist) Maximum resolution: 2-5 µm Variety of thermoplastic materials Standard materials for stamps and substrates	Very large research community, industry with increasing activity
UV-Nanoimprint Lithography (UV-NIL) a) Hard Stamp (Step and Flash) Lithography (SL) b) Soft Lithography (SL)		Resist: a) transparent (quartz) b) elastomer with hard backplate Process: Molding of liquid resin and hardening by UV-exposure Tool: a) step and repeat tool with UV-lamp b) modified mask-aligner	Similar to standard lithography (thickness contrast of a resist, UV-exposure of negative resist) Maximum resolution: 2-5 µm Fast, no heating involved	Early stage research community with increasing activity, industry
Soft Lithography (SL) – Micro-contact Printing (µCP)		Resist: Elastomers, often backed by a hard backplate Process: Transfer of an ink from the stamp surface (and from the bulk) Tool: chemical life, modified mask-aligner	Surface patterning of functional molecules possible (chemical contrast) Maximum resolution: 50 nm Easy stamp fabrication and printing Unexpensive	Beginning, fast professional tools available

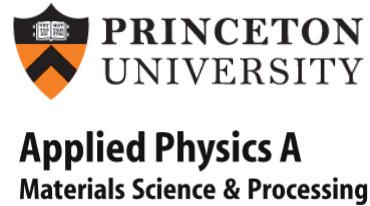
The NaPANIL Library is a guide to 3D patterning and for nanoimprint processes for applications

Printed book via
Download site:
<http://www.psi.ch/lmn/helmut-schift>

Outline

- Nanoimprint in the context of advances in mechanical engineering
- NIL is a **N**ext **G**eneration **L**ithography – true, but not only!
- Is NIL More Moore or More than Moore?
- Non-IC applications, more than Moore – front runners
- What a researcher can contribute
- ... and **More NIL** to come

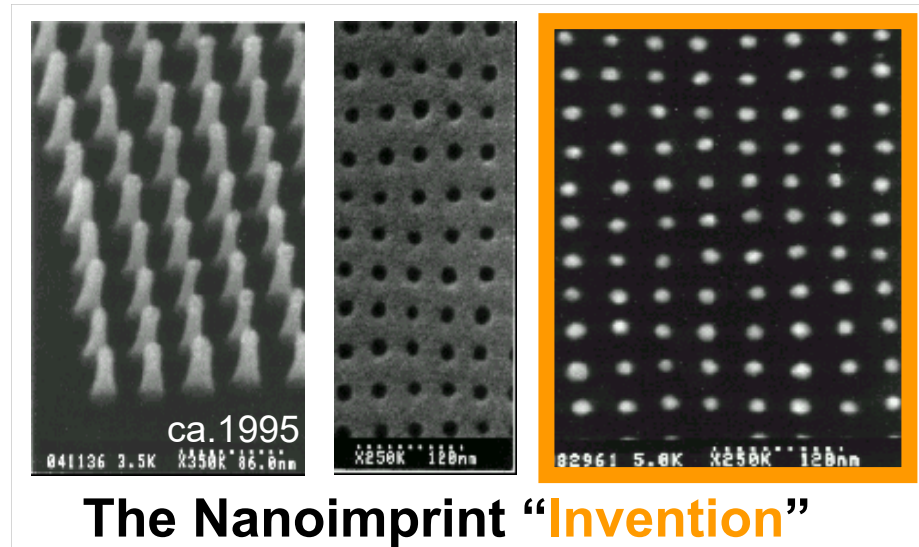
20 Years of Nanoimprint lithography (1995-2015)



Stephen Y. Chou, Princeton

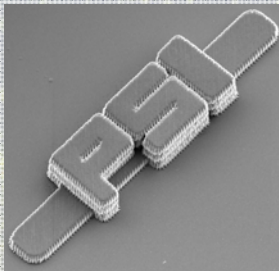
“Looking forward, clearly it is just a beginning in nanoimprint. Nanoimprint will continue to grow rapidly in academic research, making new discoveries and inventions, will exponentially grow in many industrial sectors (existing ones and future new adopters) and in revenue, and will have increasingly greater impact to modern technologies and our society. If the history of nanoimprint is any indication, we have not seen anything yet..”

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- V. Guzenko
- Nachiappan Chidambaram



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M. Vogler (mrt) and M. Altana



...

and all our colleagues in partner institutes and companies

